

3.8V

G c c i G h d c

c h h A F i h c

HI F G

- EMI Reduction with Switching Node Ringing-free
- 500kHz Switching Frequency with 6% Frequency Spread Spectrum FSS
- Pulse Skipping Mode PSM with 20uA Quiescent Current in Light Load Condition
- 3.8V-32V Wide Input Voltage Range
- Up to 2A Continuous Output Load Current
- 0.8V $\pm 1\%$ Feedback Reference Voltage
- Fully Integrated 130 $R_{ds(on)}$ High Side MOSFET and 70 $R_{ds(on)}$ Low Side MOSFET
- 1uA Shut-down Current
- 80ns Minimum On-time
- Precision Enable Threshold for Programmable UVLO Threshold and Hysteresis
- Low Dropout Mode Operation
- 4ms Built-in Soft Start Time
- Output Over Voltage Protection
- Thermal Shutdown Protection at 160°C
- Available in TSOT23-6L Package

DD HCBG

- White Goods, Home Appliance
- Surveillance
- Audio, WiFi Speaker
- Printer, Charging Station
- DTV, STB, Monitor/LCD Display

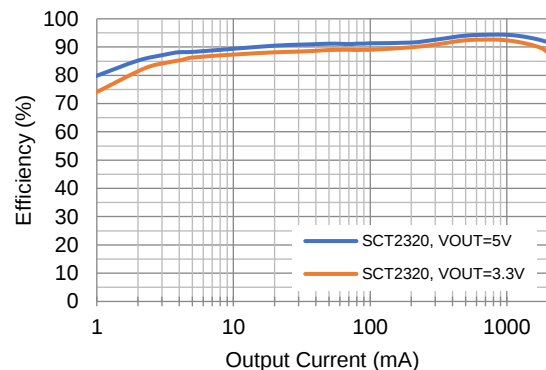
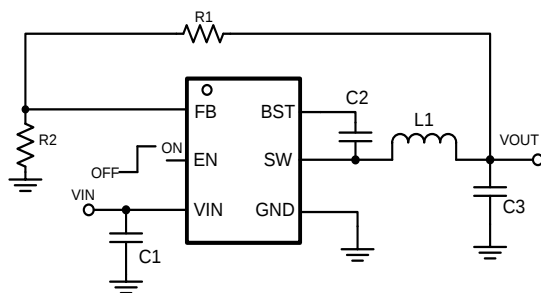
G F DHCB

The SCT2320 is 2A synchronous buck converters with up to 32V wide input voltage range, which fully integrates a 130 $R_{ds(on)}$ high-side MOSFET and a 70 $R_{ds(on)}$ low-side MOSFET to provide high efficiency step-down DCDC conversion. The SCT2320 adopts peak current mode control with the integrated compensation network, which makes SCT2320 easily to be used by minimizing the off-chip component count. The SCT2320 supports the Pulse Skipping Modulation (PSM) with typical 20uA Ultra-Low Quiescent and achieves more than 80% efficient at 1mA and 88% at 5mA light load conditions.

The SCT2320 is an Electromagnetic Interference (EMI) friendly buck converter with implementing optimized design for EMI reduction. The SCT2320 features Frequency Spread Spectrum FSS with $\pm 6\%$ jittering span of the 500kHz switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI. The converter has proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching.

The SCT2320 offers output over-voltage protection, cycle-by-cycle peak current limit, and thermal shutdown protection. The device is available in a low-profile TSOT23-6L package.

HMD DD HCB



SCT2320

F 2G2CB 2GHCFM

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.1: Released to Production. Add orderable part number information.

Revision 1.2: Delete VS in ABS table

Revision 1.3: Update Device Order Information

2 CF F 2B CFA H2CB

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION
SCT2320TVBR	Tape & Reel	3000	2320	6	TSOT23-6L

GC IH A L2AIA F H2B G

D2B CB 2 IF H2CB

Over operating free-air temperature unless otherwise noted⁽¹⁾

DESCRIPTION

MIN

BST	6	Power supply for the high-side power MOSFET gate driver. Must connect a 0.1uF or greater ceramic capacitor between BST pin and SW node.
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SCT2320

F CAA B CD F H2B CB 2H2CBG

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V _{IN}	Input voltage range	3.8	32	V

V_{IN}=12V, T_J=-40°C~125°C, typical values are tested under 25°C.

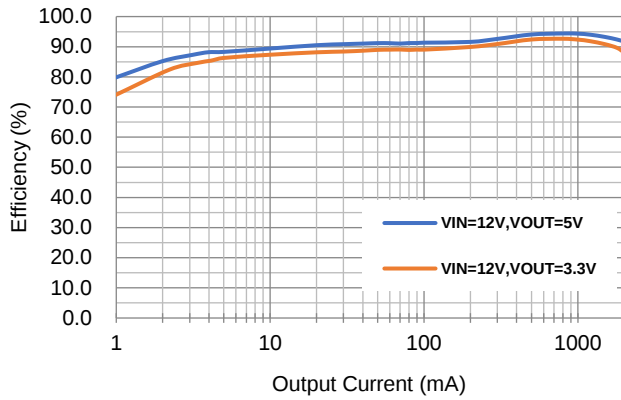


Figure 1. SCT2320 Efficiency, Vin=12V

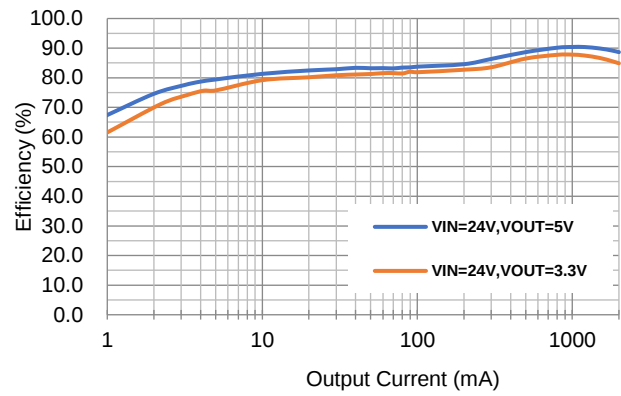


Figure 2. SCT2320 Efficiency, Vin=24V

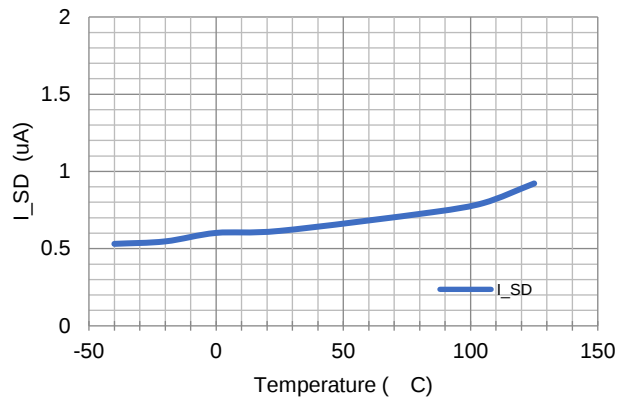


Figure 3. Shut-down Current vs Temperature

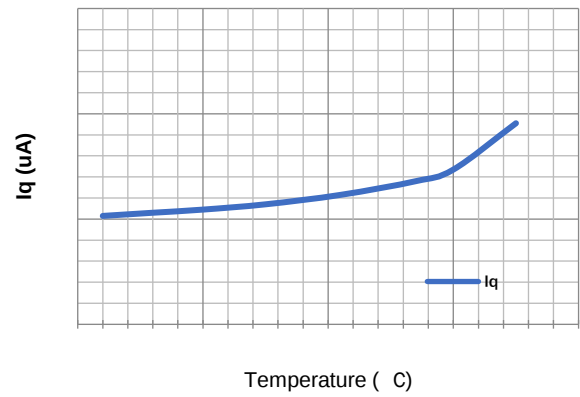


Figure 4. Quiescent Current vs Temperature

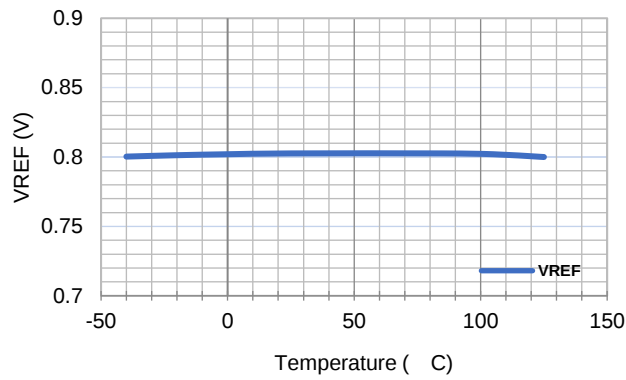


Figure 5. Reference Voltage vs Temperature

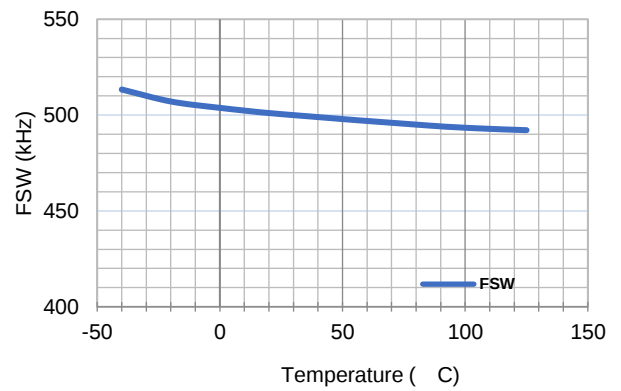


Figure 6. Center Switching Frequency vs Temperature

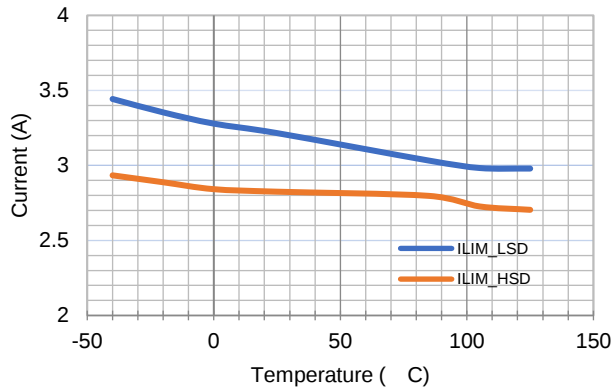


Figure 7. Peak Current Limit vs Temperature

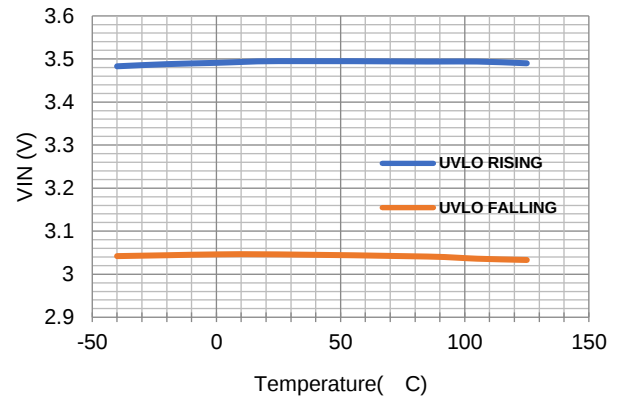


Figure 8. VIN UVLO vs Temperature

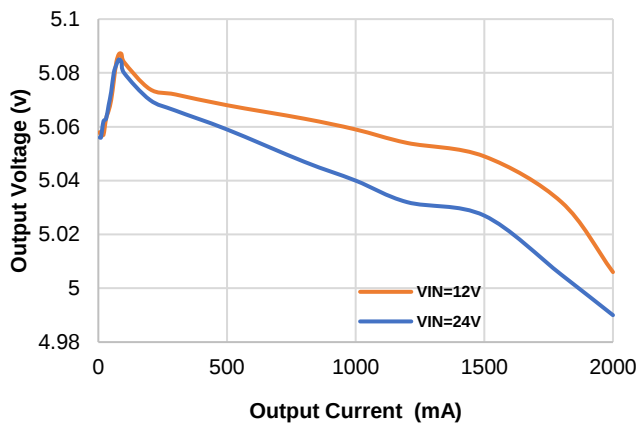


Figure 9. Load Regulation (VOUT=5V)

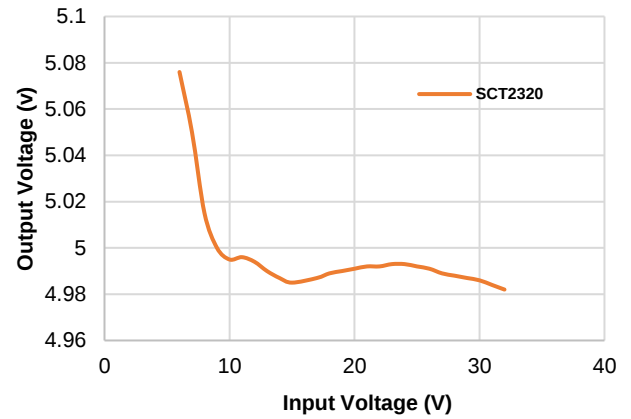
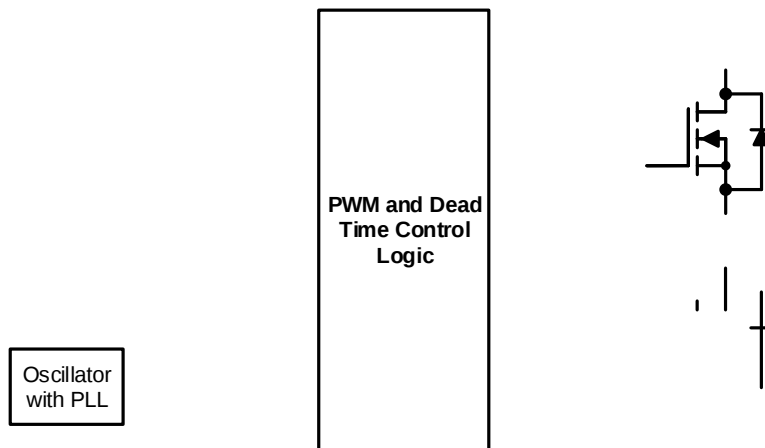


Figure 10. Line Regulation (IOUT=2A)

I B H C B C ? F A

EN

FB



CD F HCB

Overview

The SCT2320 device is 3.8V-32V input, 2A output, EMI friendly, fully integrated synchronous buck converters. The device employs fixed frequency peak current mode control. An internal clock with 500kHz frequency initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly and the converter charges output cap. When sensed voltage on high-side MOSFET peak current rising above the voltage of internal COMP (see functional block diagram), the device turns off high-side MOSFET Q1 and turns on low-side MOSFET Q2. The inductor current decreases when MOSFET Q2 is ON. In the next rising edge of clock cycle, the low-side MOSFET Q2 turns off. This repeats on cycle-by-cycle based.

The peak current mode control with the internal loop compensation network and the built-in 4ms soft-start simplify the SCT2320 footprints and minimize the off-chip component counts.

The error amplifier serves the COMP node by comparing the voltage on the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The quiescent current of SCT2320 is 20uA typical under no-load condition and no switching. When disabling the device, the supply shut down current is only 1 . The SCT2320 works at Pulse Skipping Mode PSM to further increase the power efficiency in light load condition, hence the power efficiency can be achieved up to 88% at 5mA load condition.

The SCT2320 implements the Frequency Spread Spectrum FSS modulation spreading of $\pm 6\%$ centered 500kHz switching frequency. FSS improves EMI performance by not allowing emitted energy to stay in any one receiver band for a significant length of time. The converter has optimized gate driver scheme to achieve switching node voltage ringing-free without sacrificing the MOSFET switching time to further damping high frequency radiation EMI noise.

The hiccup mode minimizes power dissipation during prolonged output overcurrent or short conditions. The hiccup wait time is 512 cycles and the hiccup restart time is 8192 cycles. The SCT2320 device also features full protections including cycle-by-cycle high-side MOSFET peak current limit, over-voltage protection, and over-temperature protection.

VIN Power

The SCT2320 is designed to operate from an input voltage supply range between 3.8V to 32V, at least 0.1uF decoupling ceramic cap is recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional electrolytic or tantalum bulk capacitor or with recommended 22uF may be required in addition to the local ceramic bypass capacitors.

Under Voltage Lockout UVLO

The SCT2320 Under Voltage Lock Out (UVLO) default startup threshold is typical 3.5V with VIN rising and shutdown threshold is 3.1V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin.

Enable and Start up

When applying a voltage higher than the EN high threshold (typical 1.18V/rise), the SCT2320 enables all functions

and the device starts soft-start phase. The SCT2320 has the built in 4ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.1V/fall).

An internal 1.5uA pull up current source connected from internal LDO power rail to EN pin guarantees that floating EN pin automatically enables the device. For the application requiring higher VIN UVLO voltage than the default setup, there is a 4uA hysteresis pull up current source on EN pin which configures the VIN UVLO voltage with an off-chip resistor divider R3 and R4, shown in Figure 11. The resistor divider R3 and R4 are calculated by equation (1) and (2).

EN pin is a high voltage pin, and can be directly connected to VIN to automatically start up the device with VIN rising to its internal UVLO threshold.

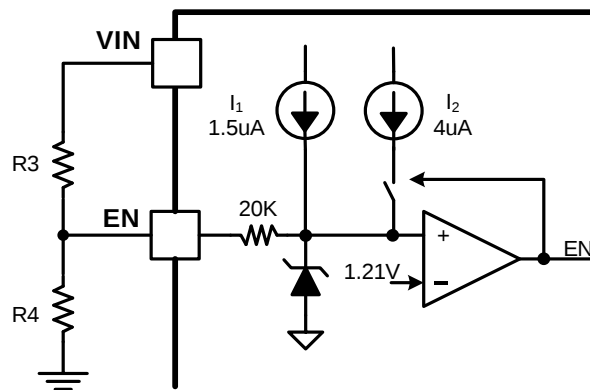


Figure 11. Adjustable VIN UVLO

$$\begin{aligned} R3 &= \frac{V_{ENR} - V_{EMF}}{I_1} \quad (1) \\ R4 &= \frac{V_{ENR} - V_{EMF}}{I_2} \quad (2) \end{aligned}$$

Where:

Vstart: Vin rise threshold to enable the device

Vstop: Vin fall threshold to disable the device

$I_1=1.5\mu A$

$I_2=4\mu A$

$V_{ENR}=1.18V$

$V_{EMF}=1.1V$

EMI Reduction with Frequency Spread Spectrum and Switching Node Ringing-free

In some applications, the system EMI test must meet EMI standards EN55011 and EN55022. To improve EMI performance, SCT2320 adopts Frequency Spread Spectrum (FSS) to spread the switching noise over a wider band and therefore reduces conducted and radiated interference peak amplitude at particular frequency. The SCT2320 features 500kHz switching frequency with spreading frequency of +/-6% and modulation rate 1/512 of switching

frequency. The FSS technique effectively decreases the EMI noise by spreading the switching frequency from fixed 500kHz to a range 517kHz ~ 583kHz. As a result, the harmonic wave amplitude is reduced and the harmonic wave band is wider.

In buck converter, the switching node ringing amplitude and cycles are critical especially related to the high frequency radiation EMI noise. The SCT2320 implements the multi-level gate driver speed technique to achieve the switching node ringing-free without sacrificing the switching node rise/fall slew rate and power efficiency of the converter. The switching node ringing amplitude and cycles are damped by the built-in MOSFETs gate driving technique (SCT Patented Proprietary Design). The switching node zoomed in wave form is shown in Figure 12.

Figure 12. SCT2320 Switching Node Waveform

Figure 13. SCT2320 LDO Mode Waveform

Peak Current Limit and Hiccup Mode

The SCT2320 has cycle-by-cycle peak current limit with sensing the internal high side MOSFET Q1 current during overcurrent condition. While the Q1 turns on, its conduction current is monitored by the internal sensing circuitry. Once the high-side MOSFET Q1 current exceeds the limit, it turns off immediately. If the Q1 over current time exceeds 512 switching cycles (hiccup waiting time), the buck converter enters hiccup mode and shuts down. After 8192 cycles off, the buck converter restarts to power up. The hiccup modes reduce the power dissipation in over current condition.

Over Vo

(PSM) mode to increase the converter power efficiency at light load condition. When the inductor current decreases to zero, zero-cross detection circuitry on high-side MOSFET Q1 forces the Q1 off till the beginning of the next switching cycle. The buck converter does not sink current from the load when the output load is light and converter works in PSM mode.

Bootstrap Voltage Regulator

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

The floating supply (BST to SW) UVLO threshold is 2.7V rising and hysteresis of 350mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.35V, BST UVLO occurs. The SCT2320 intervenes to turn on low side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee operation over a wide duty range.

Low Drop-out Regulation

To support the application of small voltage-difference between Vout and Vin, the Low Drop Out (LDO) Operation is implemented by the SCT2320. The Low Drop Out Operation is triggered automatic when the off time of the high-side power MOSFET exceeds the minimum off time limitation.

In low drop out operation, high-side MOSFET remains ON as long as the BST pin to SW pin voltage is higher than BST UVLO threshold. When the voltage from BST to SW drops below 2.35V, the high-side MOSFET turns off and low-side MOSFET turns on to recharge bootstrap capacitor periodically in the following several switching cycles. Only 100ns of low side MOSFET turning on in each refresh cycle minimizes the output voltage ripple. Low-side MOSFET may turn on for several times till bootstrap voltage is charged to higher than 2.7V for high-side

MOSFET working normally. Then high-side MOSFET turns on and remains on until bootstrap voltage drops to trigger bootstrap UVLO again. Thus, the effective duty cycle of the switching regulator during Low Drop-out LDO operation can be very high even approaching 100% as shown in Figure 13.

DD 2 HCB 2B CFA HCB

Typical Application

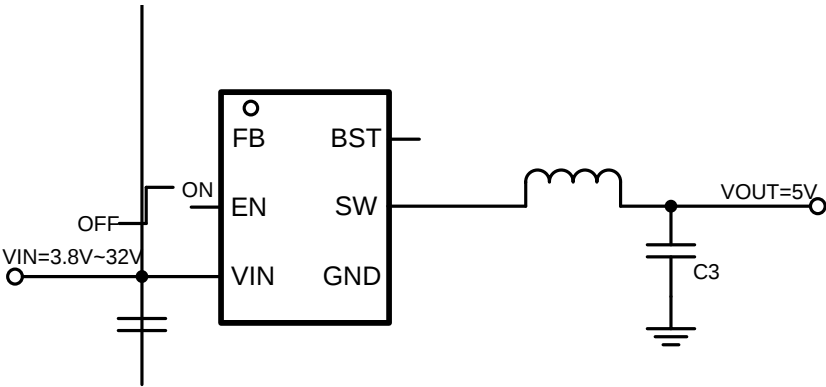


Figure 14. 24V Input, 5V/2A Output

Design Parameters

Design Parameters	Example Value
Input Voltage	24V
Output Voltage	5V
Output Current	2A
Output voltage ripple (peak to peak)	±0.3V
Switching Frequency	500kHz

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10 μ F is recommended for the decoupling capacitor and should be placed as close as possible to the VIN pin of the SCT2320.

Use Equation (3) to calculate the input voltage ripple:

(3)

Where:

- C_{IN} is the input capacitor value
- f_{SW} is the converter switching frequency
- I_{OUT} is the maximum load current

Due to the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the VIN pin. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, a 35V/10 μ F input ceramic capacitor is recommended for most of applications. Choose the right capacitor value carefully with considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Inductor Selection

The performance of the buck converter is affected by the inductor value, DC resistance (DCR), and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DCR, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have $\pm 20\%$ or even $\pm 30\%$ tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the maximum input voltage, minimum output voltage, maximum load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a buck converter, calculate the inductor minimum value as shown in equation (4).

(4)

Where:

- K_{IND} is the coefficient of inductor ripple current relative to the maximum output current.

Therefore, the peak switching current of inductor, I_{LPEAK} , is calculated as in equation (5).

(5)

Set the current limit of the SCT2320 higher than the peak current I_{LPEAK} and select the inductor with the saturation current higher than the current limit. The core loss significantly affects the efficiency of power conversion. Core loss is related to the core material and different inductors have different core

loss. For a certain inductor, larger current ripple generates higher DCR and ESR conduction losses and higher core loss.

Table 1 lists recommended inductors for the SCT2320. Verify whether the recommended inductor can support the user's target application with the previous calculations and bench evaluation. In this application, the WE's inductor 744314101 is used on SCT2320 evaluation board.

Table 1. Recommended Inductors

Part Number	L (μ H)	DCR Max (m Ω)	Saturation Current/Heat Rating Current (A)	Size Max (LxWxH mm)	Vendor
744314101	10	33	3.5	7x7x5	Würth Elektronik

Application Waveforms

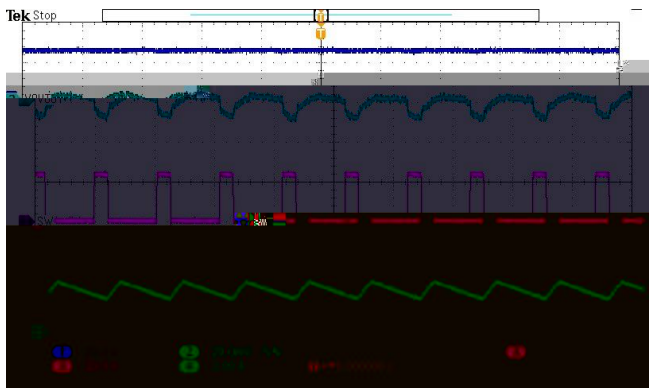


Figure 15. SW node waveform and Output Ripple
VIN=24V, IOUT=2A

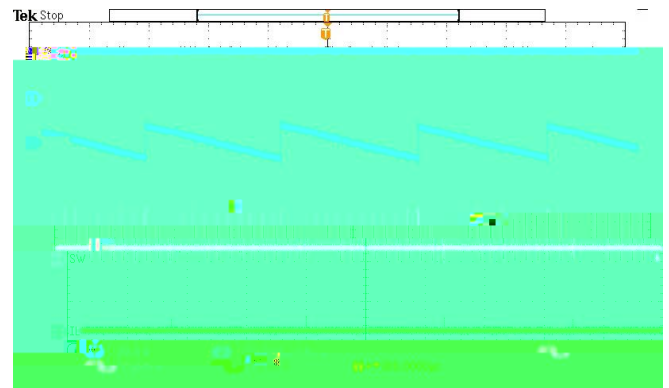


Figure 16. SW node Waveform and Output Ripple
VIN=24V, IOUT=10mA



Figure 17. Power Up
VIN=24V, VOUT=5V, IOUT=2A

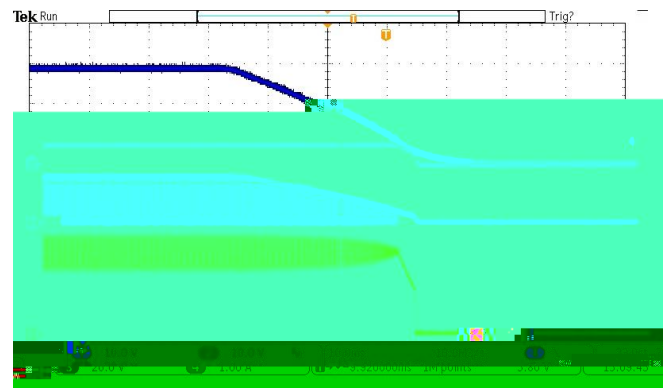


Figure 18. Power Down
VIN=24V, VOUT=5V, IOUT=2A

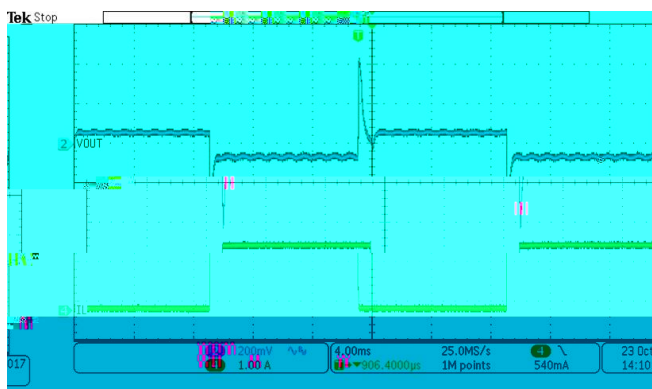


Figure 19. Load Transient
VOUT=5V, IOUT=0.2A to 1.8A, SR=250mA/us

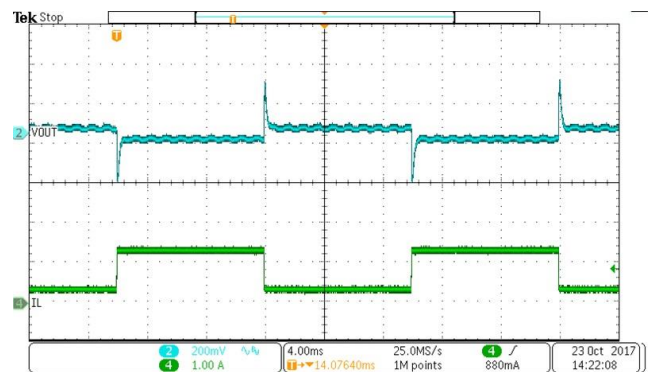


Figure 20. Load Transient
VOUT=5V, IOUT=0.5A to 1.5A, SR=250mA/us

Layout Guideline

The regulator could suffer from instability and noise problems without carefully layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be very close to the VIN pin and GND pin to reduce the input supply ripple. Place the capacitor as close to VIN pin as possible to reduce high frequency ringing voltage on SW pin as well. Figure 21 is the recommended PCB layout of SCT2320.

The layout needs be done with well consideration of the thermal. A large top layer ground plate using multiple thermal vias is used to improve the thermal dissipation. The bottom layer is a large ground plane connected to the top layer ground by vias.

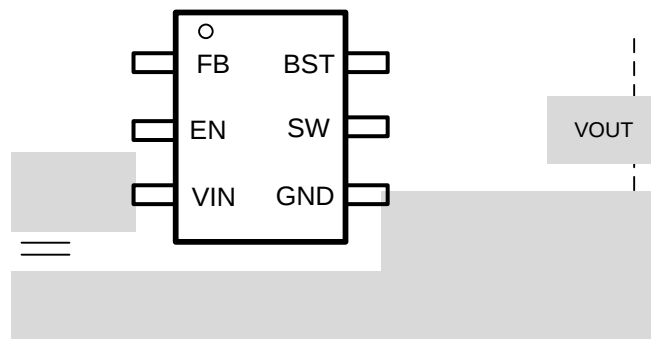


Figure 21. PCB Layout Example

Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation (12).

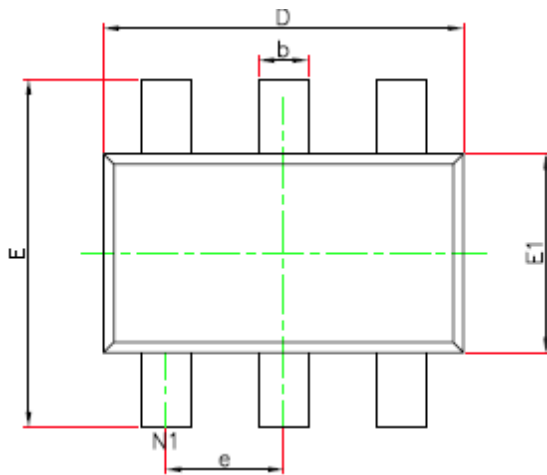
$$P_{D(max)} = \frac{T_J - T_A}{R_{JA}} \quad (12)$$

where

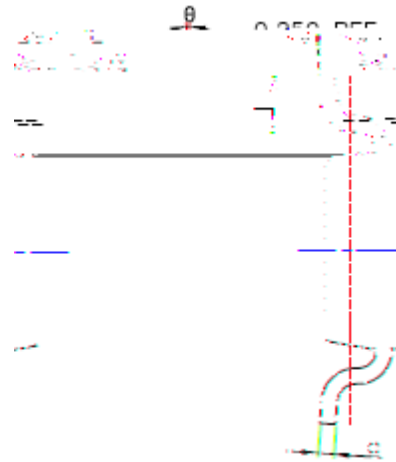
- T_A is the maximum ambient temperature for the application.
- R_{JA} is the junction-to-ambient thermal resistance given in the Thermal Information table.

The real junction-to-ambient thermal resistance R_{JA} of the package greatly depends on the PCB type, layout, thermal pad connection and environmental factor. Using thick PCB copper and soldering the GND to a large ground plate enhance the thermal performance. Using more vias connects the ground plate on the top layer and bottom layer around the IC without solder mask also enhance the thermal capability.

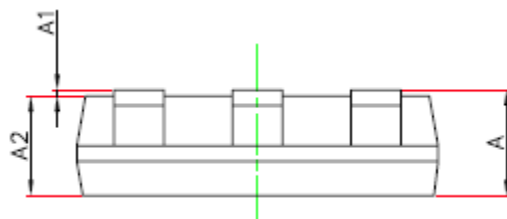
D B CFA HCB



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	-----		1.10
A1	0.000		0.10
A2	0.70		1.00
D	2.85		2.95
E	2.65		2.95
E1	1.55		1.65
b	0.30		0.50
c	0.08		0.20
e	0.95(BSC)		
L	0.30		0.60
	0		8

F H D FHG

PN	DESCRIPTION	COMMENTS
SCT2325 SCT2323	3.8V-32V Vin, Fixed Vout, 2A Synchronous Buck Converter with EMI Reduction	• 1.1MHz switching frequency with $\pm 6\%$ FSS • EMI reduction with switching node ringing-free. • SW anti-ringing in discontinuous current mode • 20uA ultra-low quiescent current • Minimum external components. Easy-to-use • Fixed 5V Vout (SCT2325) and 3.3V Vout (SCT2323)
SCT2330 SCT2331	3.8V-32V Vin, 3A Synchronous Step-down DCDC Converter with EMI Reduction	• 500KHz switching frequency • 3A Continuous output current • EMI reduction with switching node ringing-free. • Ultra-low quiescent current. High efficiency PFM at light load (SCT2330) • Frequency Spread Spectrum (SCT2330) • Fixed PWM mode for lower output ripple (SCT2331)

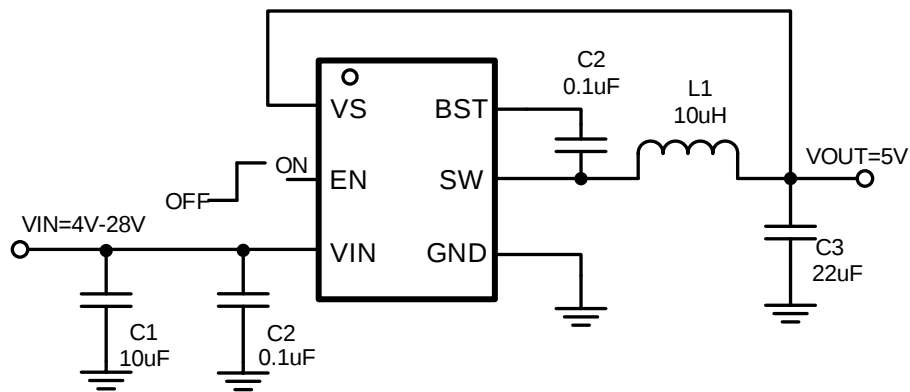


Figure 22. SCT2325 Typical Application

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