Qualified for Automotive Applications
AEC-Q100 Qualified with the Following Results:
- Device Temperature Grade 1

Wide Input Voltage Range: 3.5V-36V

One Synchronous HV Buck Converter VOUT1:
- Up to 3A Continuous Output Current
- Output Voltage of 3.3/3.7/4.6/5V

Dual Synchronous LV Buck Converters VOUT2, VOUT3:
- Up to 2A Continuous Output Current
- Output Voltage Range 0.8V to 2.35V with 50mV Steps

One Low-Drop Regulator(LDO) VOUT4:
- Up to 400mA Continuous Output Current
- Output Voltage: 1.8/2.7/2.8/2.9/3.3V

+/- 1.5% Feedback Reference Voltage

Fixed 2.1MHz

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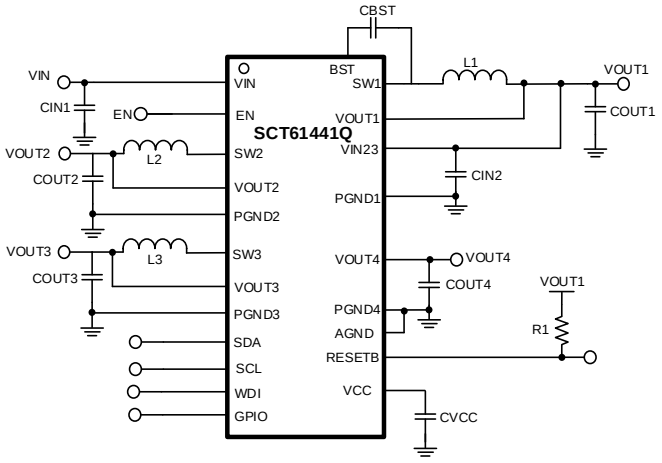
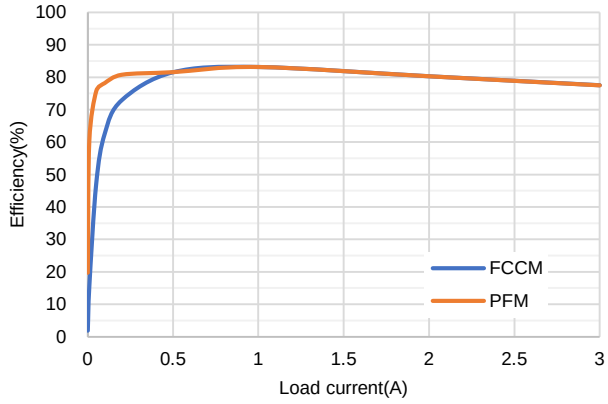
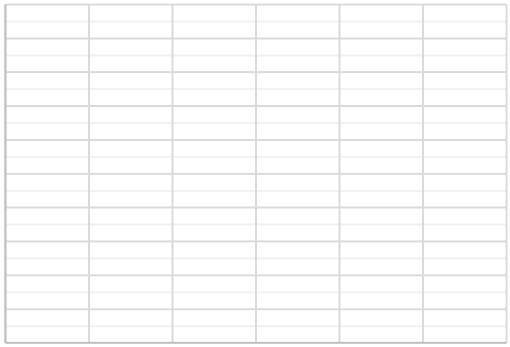


SCT61441Q PMIC Typical Application Circuit



Buck1 Efficiency vs Load Current, V_{OUT1}=3.3V, f_{SW1}=2.1MHz



Buck1 Efficiency vs Load Current, V_{OUT1}=3.3V, f_{SW1}=400kHz

Buck2/3 Efficiency vs Load Current, $V_{OUT2/3}$=1.2V

NAME	NO.	DESCRIPTION
VOUT1	14	Voltage sense for the output of Buck1. The device regulates VOUT1 voltage to the setting value. The device regulates VOUT1 voltage to the value of 3.3V typical. Connect this pin to HV Buck1 output voltage via short trace.
PGND1	15	Power ground pin of HV Buck1.
SW1	16	Regulator switching node of HV Buck1. Connect SW1 to an external power inductor
VIN	17	Input supply voltage. Connect a local bypass capacitor from VIN pin to GND pin. Path from VIN pin to high frequency bypass capacitor and GND must be as short as possible.
BST	18	Power supply bias for high-side power MOSFET gate driver of Buck1. Connect a 0.1uF capacitor from BST pin to SW pin. Bootstrap capacitor is charged when low-side power MOSFET is on or SW voltage is low.
EN	19	Enable pin. All four outputs will be activated once voltage upon EN reaches high threshold. The input voltage lockout threshold can be adjusted by connecting this pin to the input voltage through a resistor divider. The EN pin is internally pulled-down through 2.1M resistor. Connect to VIN pin if not used.
VCC	20	Output of the internal VCC regulator. Connect a ceramic bypass capacitor from this pin to PGND.
AGND	21	Analog ground pin of device. Connect this pin to power ground directly.
NC	22, 23	Not connected. Connect NC pins to ground.
PGND4	24	Power ground pin. Connect this pin to other PGND pins.

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Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{IN}	Input voltage range	3.5	36	V
V_{OUT2}	LV Buck2 output voltage range	0.8	2.35	V
V_{OUT3}	LV Buck3 output voltage range	0.8	2.35	V
V_{OUT4}	LDO output voltage range	1.8	3.3	V
T_J	Operating junction temperature	-40	150	°C

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per AEC-Q100-002	-2	+2	kV
	Charged Device Model(CDM), per AEC-Q100-011	-1	+1	kV

PARAMETER	THERMAL METRIC	FCTQFN-24	UNIT
R	Junction to ambient thermal resistance(1)	39.68	°C/W
JT	Junction-to-top characterization parameter	1.78	
JB	Junction-to-board characterization parameter(1)	3.26	
R (top)	Junction to case (top) thermal resistance(1)	24.67	
R B	Junction to board thermal resistance(1)	3.46	

(1) SCT provides R and R numbers only as reference to estimate junction temperatures of the devices. R and R are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT61441Q is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT61441Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual R and R .

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V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		3.5		36	V
$V_{IN\_UVLO\_RISING}$	Input UVLO rising threshold	VIN_START[1:0]=00b	3	3.2	3.4	V
		VIN_START[1:0]=01b	3.8	4	4.2	V
		VIN_START[1:0]=10b	4.8	5	5.2	V
		VIN_START[1:0]=11b	5.8	6	6.2	V
$V_{IN\_UVLO\_FALLING}$	Input UVLO falling threshold	VIN_STOP[1:0]=00b	2.5	2.8	3.1	V
		VIN_STOP[1:0]=01b	3.2	3.5	3.8	V
		VIN_STOP[1:0]=10b	4.2	4.5	4.8	V
		VIN_STOP[1:0]=11b	5.2	5.5	5.8	V
V_{IN_OVP}	Input OVP	V_{IN} rising	40	43	45	V
$V_{IN\_OVP\_HYS}$ 4B	Hysteresis			3		V
I_{SD}	Shutdown current					

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V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
R_{DSON_H1}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=5V		75	150	m
R_{DSON_L1}	Low-side MOSFET on-resistance			50	120	m
I_{LIM_HS1}	High-side power MOSFET current limit		4.2	5.2	6.2	A
I_{LIM_LSP1}	Low-side power MOSFET positive current limit		3.2	4.2	5.2	A
I_{LIM_LSN1}	Low-side power MOSFET negative current limit		0.8	2	3.2	A
R_{DIS1}	Discharge resistance	Output disabled		100	200	
t_{ON_MIN1}	Minimum on-time			80		ns
$_{Phase1}$(1)	Switching phase			0		deg
VOUT2 (LV Buck)						
V_{S2}(1)	Supply voltage range		3		5.5	V
V_{ACC2}	Voltage accuracy	T_J = 25°C	-1		1	%
		T_J = -40°C~150°C	2		2	%
R_{DSON_H2}	High-side MOSFET on-resistance			65	150	m
R_{DSON_L2}	Low-side MOSFET on-resistance			50	120	m
I_{LIM_HS2}	High-side power MOSFET current limit		2.8	3.6	4.4	A
I_{LIM_LSP2}	Low-side power MOSFET positive current limit		2.2	3.2	4.2	A
I_{LIM_LSN2}	Low-side power MOSFET negative current limit		1	2	3	A
R_{DIS2}	Discharge resistance	Output disabled		50	100	
t_{ON_MIN2}	Minimum on-time			90		ns
$_{Phase2}$(1)	Switching phase			0		deg
VOUT3 (LV Buck)						
V_{S3}(1)	Supply voltage range		3		5.5	V
V_{ACC3}	Voltage accuracy	T_J = 25°C	-1		1	%
		T_J = -40°C~150°C	2		2	%
R_{DSON_H3}	High-side MOSFET on-resistance			65	150	m
R_{DSON_L3}	Low-side MOSFET on-resistance			50	120	m
I_{LIM_HS3}	High-side power MOSFET current limit		2.8	3.6	4.4	A
I_{LIM_LSP3}	Low-side power MOSFET positive current limit		2.2	3.2	4.2	A
I_{LIM_LSN3}	Low-side power MOSFET negative current limit		1	2	3	A

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V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN

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V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{OVTH}	Output over-voltage threshold for all outputs	PG1/2/3/4_SEL[1:0]=01, VOUT rising		106		%
		Hysteresis		2		%
V_{UVTH}	Output under-voltage threshold for all outputs	PG1/2/3/4_SEL[1:0]=01, VOUT falling		94		%
		Hysteresis		2		%
V_{DOVPTH}	Output deep over-voltage threshold for all outputs	DEEP_OVP_SEL[1:0]=00, VOUT rising	110	115	120	%
		Hysteresis		2		%
V_{DUVPTH}	Output deep under-voltage threshold for all outputs	DEEP_UVP_SEL[1:0]=00,VOUT falling	70	75	80	%
		Hysteresis		2		%
T_{HIC}(1)	Hiccup time			80		ms
T_{SD}	Thermal shutdown threshold	T_J rising		175		°C
	Hysteresis			20		°C
Watch Dog Interface						
R_{WDDIS}	WDDIS Input Pulldown	EN high		1.8		M
V_{WDI_HI}	Threshold for WDI pin	WDI voltage rising		1.2	1.4	V
V_{WDI_LO}						

314.83 in WLa 0 Tw 2 pS nID 80.454202TdTLsID 80.406202TdTL ID 87 >>BD 92 14.820

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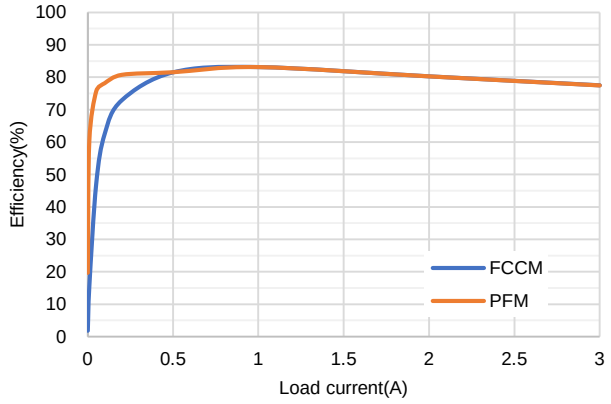
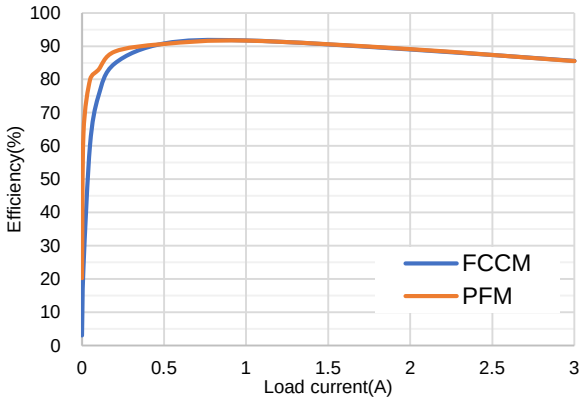
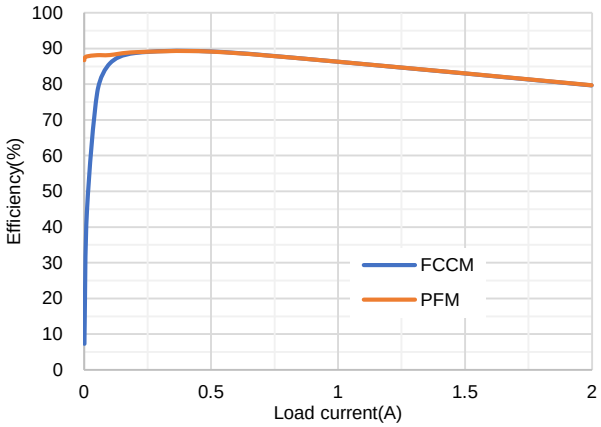
V_{IN}=12V, T_J=-40°C~125°C, unless otherwise noted.



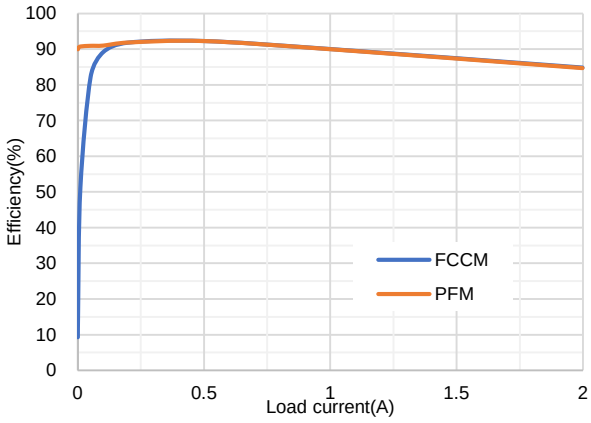
Buck1 Efficiency vs Load Current, V_{OUT1}=3.3V, f_{SW1}=2.1MHz



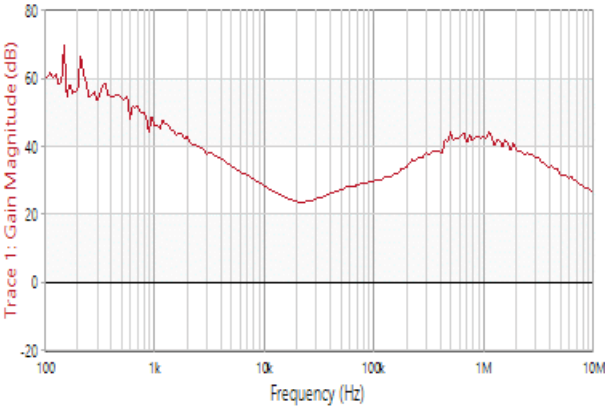
Buck1 Efficiency vs Load Current, V_{OUT1}=3.3V, f_{SW1}=400kHz



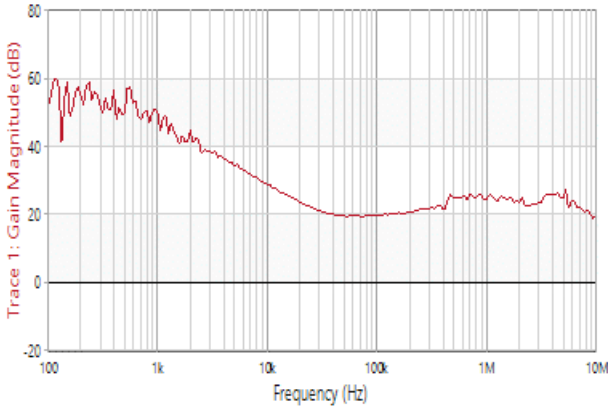
Buck2/3 Efficiency vs Load Current, $V_{OUT2/3}$=1.2V



Buck2 3 Efficiency vs Load Current, $V_{OUT2/3}$=1.8V



LDO PSRR, V_{OUT4}=2.8V, I_{OUT4}=10mA



LDO PSRR, V_{OUT4}=2.8V, I_{OUT4}=100mA

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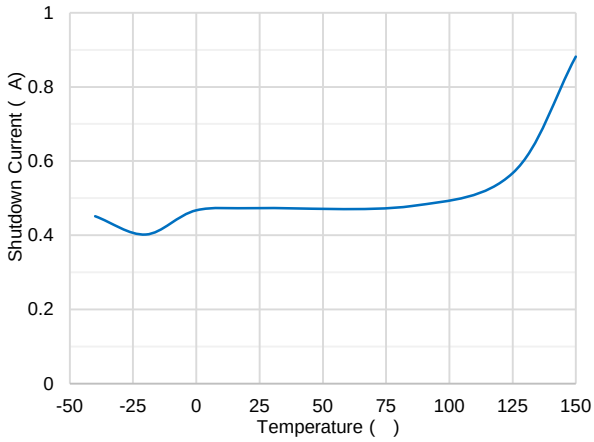
V_{IN}=12V, T_J=-40°C~125°C, unless otherwise noted.



Shutdown Current vs Temperature

UVLO Rising Threshold vs Temperature

UVLO Falling Threshold vs Temperature

VCC vs Temperature

Buck1 R_{DSON_HS1} vs Temperature

Buck1 R_{DSON_LS1} vs Temperature

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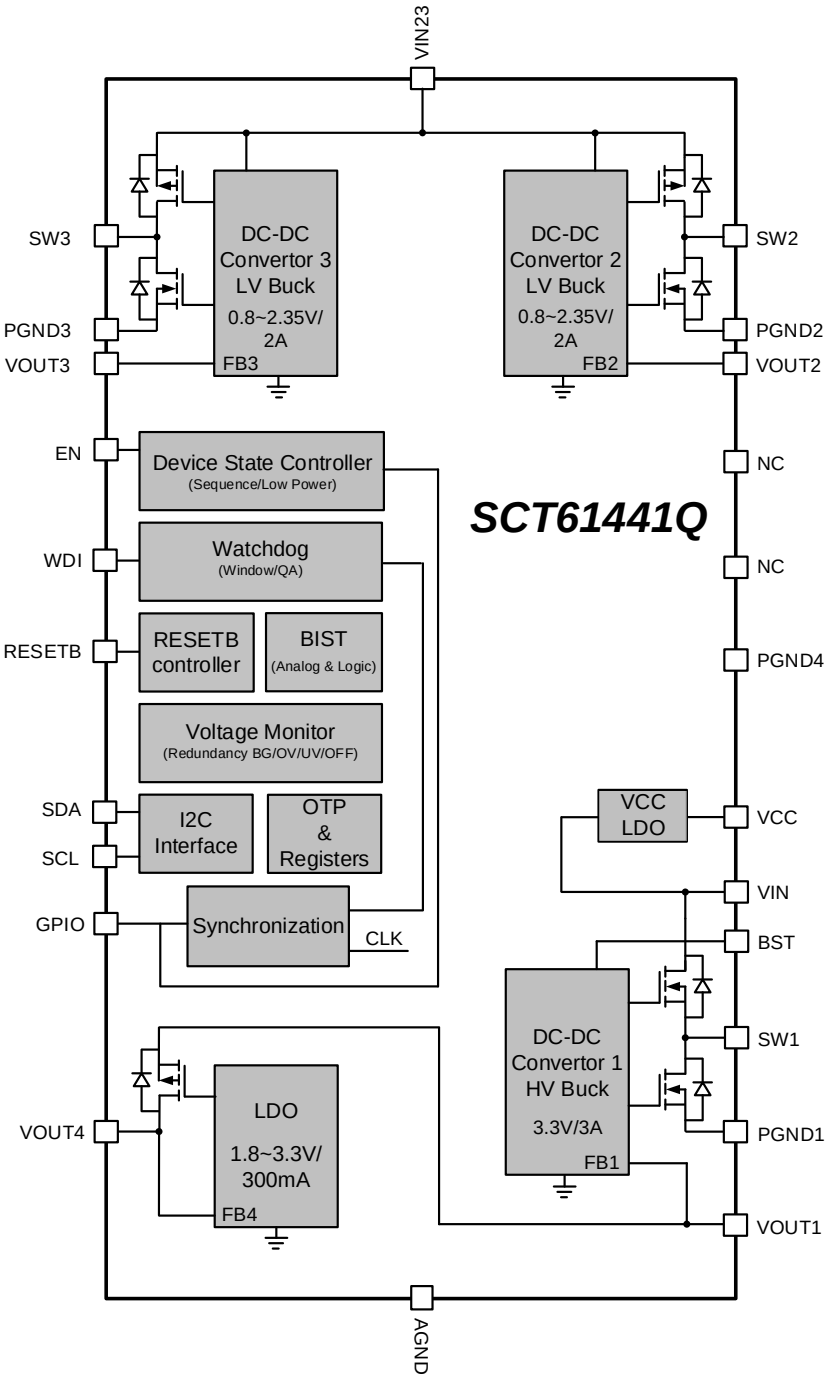

Figure 1. Functional Block Diagram

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Overview

The SCT61441Q device is a wide input power management IC with quad channels output. The device is designed for camera modules in automotive ADAS vision and DMS/OMS applications. The SCT61441Q integrates one 3A HV Buck, two identical 2A LV Buck and a 400mA LV Low-Drop Regulator(LDO). Each channel output is continuously monitored, any over-voltage/under-voltage fault will trigger RESETB pull low. Any deep over-voltage/under-voltage will be detected and the device will enter DEEPSAFE state. All output voltages are pre-programmed, which saves external feedback divider and minimizes system solution. The switching frequency of HV Buck is 2.1MHz/400kHz selectable. The switching frequency is fixed 2.1MHz for LV buck converters. The device features Frequency Spread Spectrum (FSS) with programmable jittering span of the switching frequency and modulation frequency to reduce the conducted EMI.

The device also integrates simple watchdog mode and QA watchdog mode. The dedicated WDI pin allows trigger pulse generated by MCU. Programmable watchdog window is suitable for a wide variety of applications. The RESETB output can be the sequencer of MCU to protect it from device fault.

The SCT61441Q device has protection features such as thermal shutdown, short-circuit protection and over-voltage/under-voltage protection. Disabling all outputs via I2C can reduce the quiescent current to 0.85 mA.

Operating State Machine

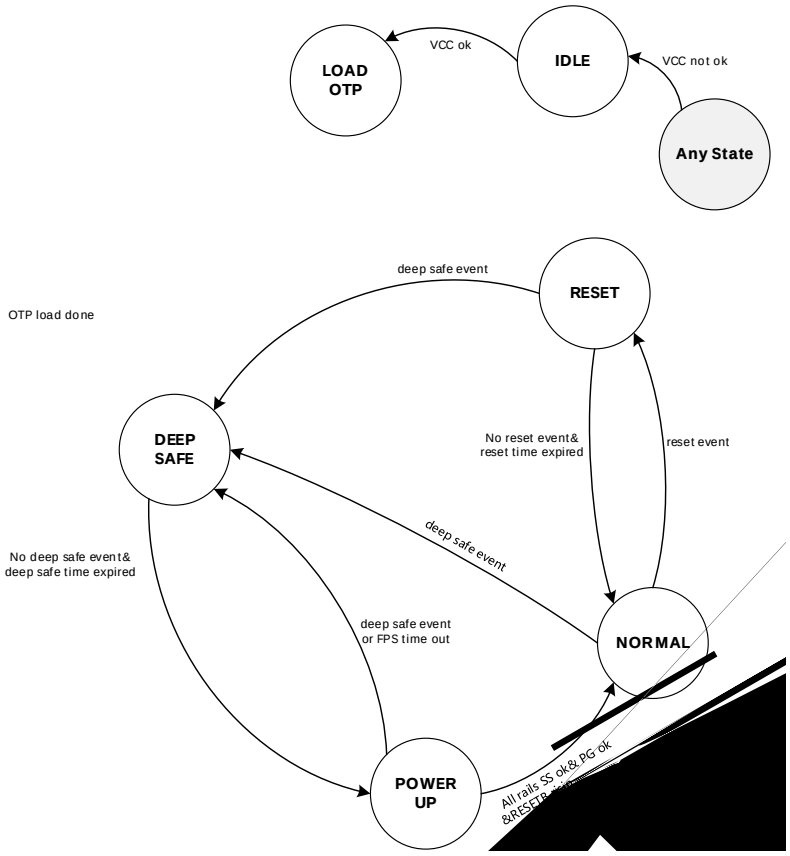

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Table 1. State and Function Matrix Table

State	Function										
	I2C	OTP load	Register reset	HV BUCK1	LV BUCK2	LV BUCK3	LDO4	Watchdog	OCP	DOVP/DUVP detect	TSD
IDLE	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
LOADOTP	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DEEPSAFE	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
POWERUP	ON	OFF	OFF	UP	UP	UP	UP	OFF	ON	ON	ON
NORMAL	ON	OFF	OFF	ON	ON	ON	ON	ON	ON	ON	ON
RESET	ON	OFF	OFF	ON	ON	ON	ON	OFF	ON	ON	ON

Table 2. State and Functional Pin Matrix Table

State	RESETB
IDLE	Tri-state
LOADOTP	LOW
DEEPSAFE	LOW
POWERUP	LOW
NORMAL	HIGH
RESET	LOW

IDLE State

The device will enter IDLE state whenever VCC is below the UVLO threshold. All functional blocks are disabled and all registers are reset. The device will exit IDLE state and jump to LOADOTP state only when VCC reaches its rising threshold 2.8V.

LOADOTP State

Once the device enters OTPLOAD state, the OTP CRC mechanism will be activated and check through all data. Only when CRC check is passed, the device will load all non-volatile memory to register. The CRC check result will be recorded in register **SYS_STATE**.

DEEPSAFE State

In DEEPSAFE state, all power rails are shut off and indicator pins are pulled low. Regardless of current state, the device will always jump to DEEPSAFE state when any deep safe event occurs. I2C interface and thermal shutdown protection are activated. MCU is able to communicate with device through I2C and read fault register to locate fault. If there is no deep safe event and deep safe timeout is expired, the device will enter POWERUP state automatically.

Deep safe events are listed as below:

VOUT1's output is out of deep OV/UV protection range or OCP

VOUT2's output is out of deep OV/UV protection range or OCP

VOUT3's output is out of deep OV/UV protection range or OCP

VOUT4's output is out of deep OV/UV protection range or OCP

Tj reaches Thermal Shutdown Point

VIN/EN UVLO

VCC OVP

VIN OVP

RESETB Stuck

Loss of ground

POWERUP State

In POWERUP state, all rails will start-up following a dedicated sequence. Since the HV buck VOUT1 is the power supply for the other channels, VOUT1 is always set to start-up first. Then the other channels will rise after turn on

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delay time respectively. The turn on delay time for each is independent and can be adjusted via changing register **CONFIG_PU1** and **CONFIG_PU2**, thus flexible sequence is available. Deep OV/UV protection is activated to protect channels from destructive OV/UV risk. If all channels finish soft-start and they are within power good range, the RESETB rising timer begins. Once the timer is expired, the device will enter NORMAL state and RESETB will output high. If deep safe event occurs, the state will transit to DEEPSAFE state directly.

NORMAL State

The NORMAL state is the normal running of device with all outputs on. The RESETB pin is released after specific delay time upon entering this state. If watchdog is enabled by register **CONFIG_WD3**, watchdog window will start after setting delay time. The delay time is configured by **WD_1UD[2:0]** in register **CONFIG_WD3**. MCU should feed the watchdog via WDI pin or write answer to specified register periodically. When operating in NOMRAL state, the device will go to RESET state once reset event occurs.

RESET State

All outputs keep on in this state, the device will transit from NORMAL state to RESET state when any of below reset event occurs:

VOUT1's output is out of OV/UV protection range

VOUT2's output is out of OV/UV protection range

VOUT3's output is out of OV/UV protection range

VOUT4's output is out of OV/UV protection rangeprotection range

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The converters have proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching.

Each output voltage is continuously monitored during operation, the OV/UV threshold can be adjusted independently in register **CONFIG_PGSEL1** and **CONFIG_PGSEL2**.

Deep Over Voltage Protection

If any output exceeds the deep over voltage protection threshold 115%, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again following turn on delay setting in register. When entry hiccup, the output discharge will operate during the hiccup time. The threshold can be configured by bits **DEEP_OVP_SEL[1:0]**.

Deep Under Voltage Protection

If an output falls below the deep under voltage protection threshold 75%, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again following turn on delay setting in register. When entry hiccup, the output discharge will operate during the hiccup time. The threshold can be configured by bits **DEEP_UVP_SEL[1:0]**.

Thermal Shutdown

The thermal shutdown protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 175°C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 155°C, the device will restart with internal soft start phase.

Over Current Protection (OCP)

The converters implement over current protection with cycle-by-cycle limiting high-side MOSFET peak current and also low-side MOSFET valley current to avoid inductor current running away during unexpected overload and hiccup protection in output hard short condition. When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement even though the inductor current has already been clamped at over current limitation. Thus, output voltage drops below regulated voltage continuously. When peak current point is kicked for continuous 32 times, the converter stops switching, the device will jump to DEEPSAFE state. The hiccup protection mode greatly reduces the average short circuit current to alleviate thermal issues and protect the regulator.

Frequency Spread Spectrum

To meet CISPR and automotive EMI compliances, the SCT61441Q implements Frequency Spread Spectrum (FSS) function. The FSS circuitry shifts the 2.1MHz switching frequency within dedicated range and period triangular or pseudo modulation. Therefore, the SCT61441Q can guarantee that the switching frequency does not drop into the 1.8MHz AM band limit.

Frequency Foldback

To avoid meeting minimum on time, the HV buck VOUT1 will reduce switching frequency actively when input voltage rising high. Other channel's frequency is unchanged.

When VIN greatly drops and minimum off time of HV buck VOUT1 is kicked, the VOUT1 enter dropout mode and also reduce its frequency to get max output.

RESETB Indicator

The RESETB indicator will assert when reset event occurs. It will reset MCU if it fails to feed watchdog, MCU then can reloading program to ensure the program run well. The RESETB pin is an open-drain output and can be connected to various I/O level through pull-up resistor. The reset event mapping to RESETB pin can be config2.4 (S)2.DC /TT

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Synchronization and Watchdog Disable

The device can be synchronized to an external clock when GPIO pin is set to SYNC. The external clock must be connected between the GPIO pin and ground. The synchronizat

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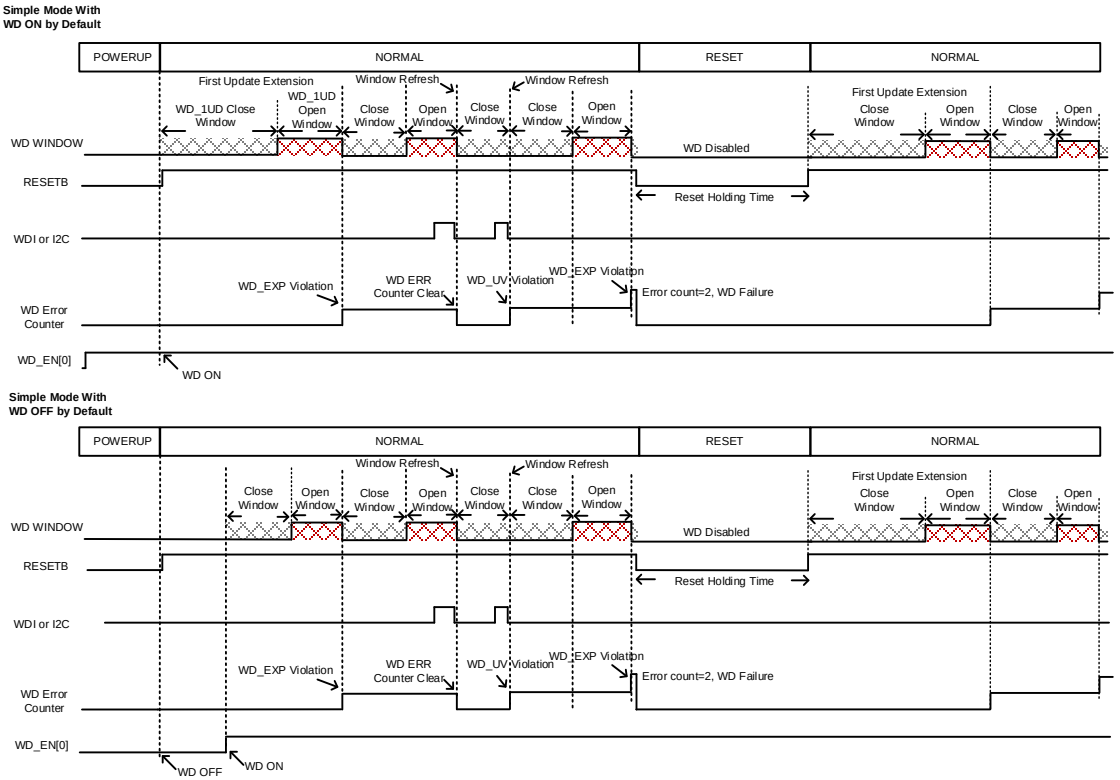
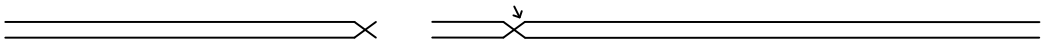


Figure 3a. Simple Watchdog Error Timing



I2C Interface

The SCT61441Q integrates a two-wire serial interface for bidirectional communications between the device and the master through bus. The I2C protocol defines two bus lines, the serial data line (SDA) and the serial clock line (SCL). The SCT61441Q is always assigned a unique chip address and operates as a slaver, the master drives the SCL line and transfer bidirectional data through SDA line. Both the SCL and SDA lines need a pull-up resistor connected to bus voltage since HIGH state is the default state when bus is idle. The SCT61441Q supports Standard-mode (up to 100 kHz), Fast-mode (up to 400 kHz), Fast-mode Plus (up to 1 MHz). The internal filtering ignores spikes and noises on the bus line to preserve data integrity. The maximum capacitive load for each bus line is given in Electrical Characteristic thus the number of interfaces is limited.

Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

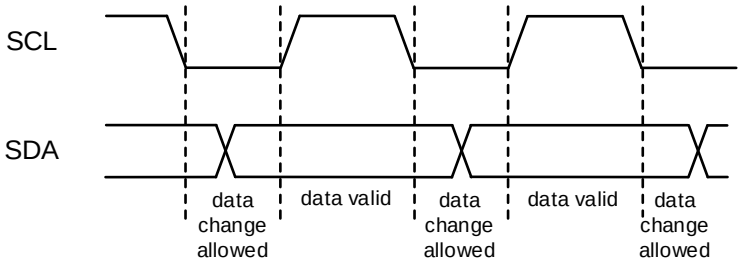


Figure 4. Data Validity Diagram

START and STOP Conditions

The data transfer always generates START and STOP conditions to announce the process. A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. Both the START and STOP conditions are generated by master on bus.

The bus is considered to be busy after START condition and released after STOP condition. A repeated START condition during transmission is also valid and will be regard as a new START condition.

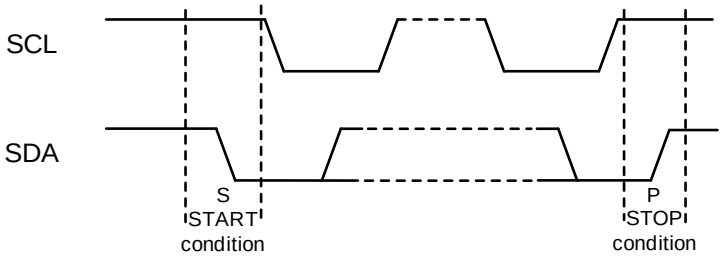


Figure 5. START and STOP Conditions Diagram

Data Transmission

The transferred byte consists of eight bits with the Most Significant Bit (MSB) first. After each byte is transferred, the master will release the SDA line and generate the ninth acknowledge clock pulse on SCL line. The SCT61441Q will pull the SDA line LOW during this acknowledge clock, to announce a successful reception and next byte may be sent. If the master is receiver and the last byte is received, it still generates the ninth acknowledge clock pulse but SDA line will not be pulled LOW. It's called not acknowledge signal and indicates the end of transmission.

After the START condition, the master must send a slave address as the first addressing byte. The slave address is seven bits long followed by an eighth R/W bit. The R/W bit defines the data direction. Set the R/W bit to 0 to indicate write command, and a 1 indicates read command. The slave address is factory-programmed between 0x38 through 0x3B, see DEVICE ORDER INFORMATION for details.

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Packet Error Checking (PEC)

The SCT61441Q supports optional packet error checking (PEC) byte during the I2C communication. PEC can significantly increase fault coverage on the I2C interface. The PEC byte is implemented through CRC-8 polynomial of x8 + x2 + x +1. The PEC byte does not take ACK, NACK, START, STOP, Repeated START bits into calculation. The PEC byte is calculated on the register address and data byte over the entire message from the first START condition, note that the slave address is removed both in write and read command. When PEC is enabled, the device will reject the write command if the master send an incorrect PEC byte. When in read mode with PEC enabled, the master should acknowledge the data byte thus then the device will send the PEC byte. The PEC can be configured by **PEC_EN** in register **CONFIG_FSS**.

Write Data Format

A write to the device includes transmission of the following:

- START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- 1 byte of data to the command register
- STOP condition

Read Data Format

A read from the device includes the following:

- Transmission of a START condition
- Slave address with the write bit set to 0
- 1 byte of data to register address
- Restart condition
- Slave address with read bit set to 1
- 1 byte of data to the command register
- STOP condition

Figure 6 illustrates the proper format for one frame.

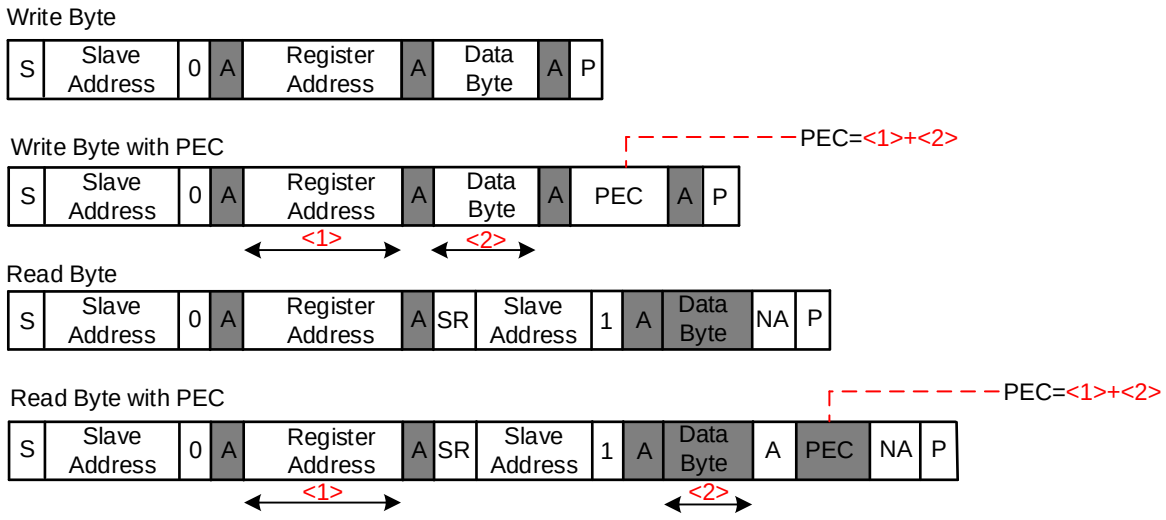

Figure 6. Transmission Data Format Diagram

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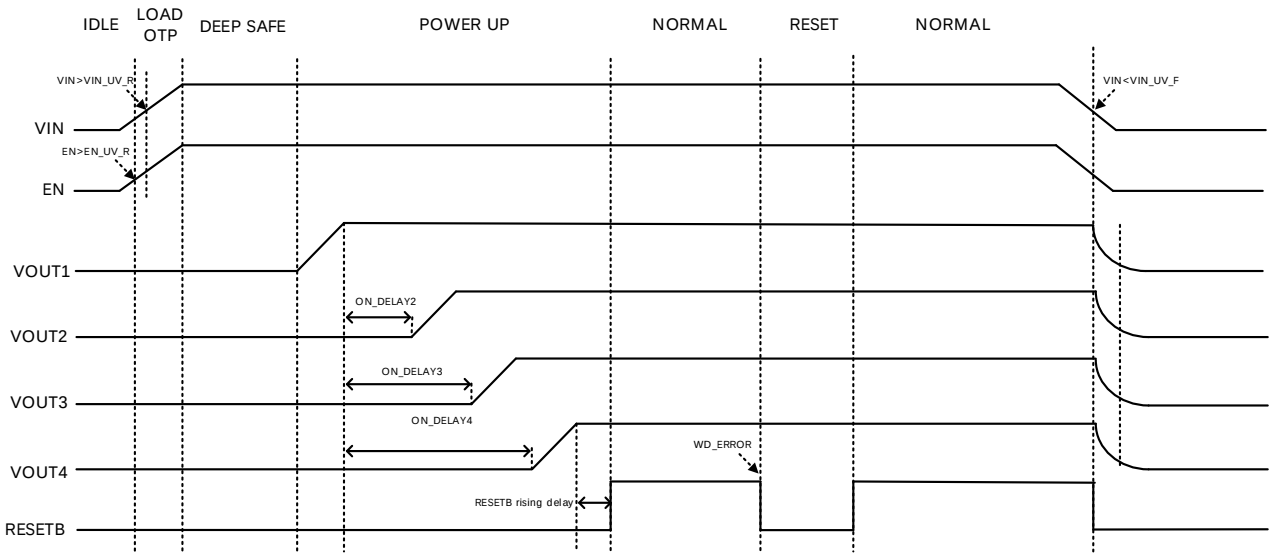

Figure 7. Power on Sequence

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Typical Application

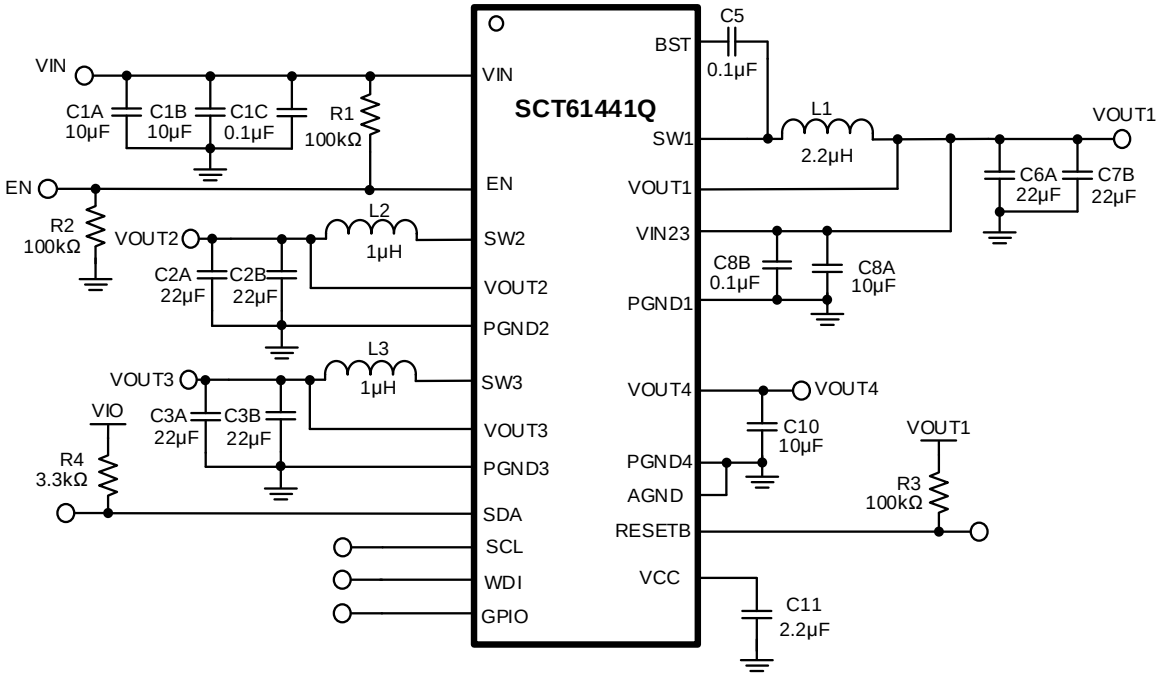

Figure 8. Application Schematic, 3.5V to 36V, PMIC Regulator at 2.1MHz

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal 3.5V to 36V
Output Voltage	VOUT1: 3.3V VOUT2: 1.2V VOUT3: 1.8V VOUT4: 2.8V
Maximum Output Current	VOUT1: 3A (in total) VOUT2: 2A VOUT3: 2A VOUT4: 400mA
Switching Frequency	2.1MHz
Output Voltage Ripple (peak to peak)	VOUT1: 10mV VOUT2: 5mV VOUT3: 5mV

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Under Voltage Lock-Out

An external voltage divider network of R_1 from the input to EN pin and R_2 from EN pin to the ground can set a higher input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. Use Equation 1 and Equation 2 to calculate the values of R_1 and R_2 resistors.

$$= 1 + \frac{1}{2} \quad (1)$$

$$= 1 + \frac{1}{2} \quad (2)$$

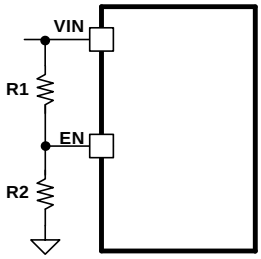

Figure 9. System UVLO by enable divide

where

V_{rise} is rising threshold of Vin UVLO

V_{fall} is falling threshold of Vin UVLO

V_{ENrise} is rising threshold of EN UVLO

V_{ENfall} is falling threshold of EN UVLO

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20%~40% of the maximum output current.

For a buck converter, the peak-to-peak ripple current in the inductor I_{LPP} can be calculated as in Equation 3.

$$= \frac{(\quad - \quad)}{} \quad (3)$$

Where

I_{LPP_BUCK} is the inductor peak-to-peak current of buck

L is the inductance of inductor

f_{SW} is the switching frequency

V_{OUT} is the output voltage

V_{IN} is the input voltage

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 4 to calculate the inductance value.

$$= \frac{}{(\quad)} \quad (1 - \frac{}{(\quad)}) \quad (4)$$

Where

L_{MIN} is the minimum inductance required

$V_{IN(max)}$ is the maximum input voltage

$I_{OUT(max)}$ is the maximum DC load current

LIR is coefficient of I_{LPP} to I_{OUT}

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The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in equation 5 and equation 6.

$$= + \frac{}{2} \quad (5)$$

$$= \sqrt{( )^2 + \frac{1}{12} ( )^2} \quad (6)$$

Where

I_{LPEAK} is the inductor peak current

I_{OUT} is the DC load current

I_{LPP} is the inductor peak-to-peak current

I_{LRMS} is the inductor RMS current

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device. The most conservative approach is to choose an inductor with a saturation current rating greater than peak current limit. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the device can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

For buck converter, the voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation 7.

$$= \sqrt{\frac{}{} (1 - \frac{}{})} \quad (7)$$

The worst case condition occurs at $V_{IN}=2*V_{OUT}$, where:

$$= 0.5 \quad (8)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 9 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta = \frac{}{} \frac{}{} (1 - \frac{}{}) \quad (9)$$

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Bootstrap Capacitor Selection

ST pin and SW1 pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

For buck converter, the output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 10 desired.

$$\Delta \quad _{-} = \frac{(\quad - \quad)}{8 \quad ^{2}} \tag{10}$$

Where

$_{OUT\_BUCK}$ is the output voltage ripple of buck converter

f_{SW} is the switching frequency

L is the inductance of inductor

C_{OUT} is the output capacitance

V_{OUT} is the output voltage

V_{IN} is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 10

Table 3. Recommended BOM for Typical Application

Output Rail	Frequency (MHz)	L (uH)	Input Capacitor (uF)	Output Capacitor (uF)
Buck1	2.1	2.2	2 x 10+1 x 0.1	2 x 22
Buck2	2.1	1	10+1 x 0.1	2 x 22
Buck3	2.1	1		2 x 22
LDO4	-	-	-	10
VCC	-	-	-	2.2

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Application Waveforms

Vin=12V, V_{OUT1}=3.3V, V_{OUT2}=1.1V, V_{OUT3}=1.5V, V_{OUT4}=2.8V, unless otherwise noted

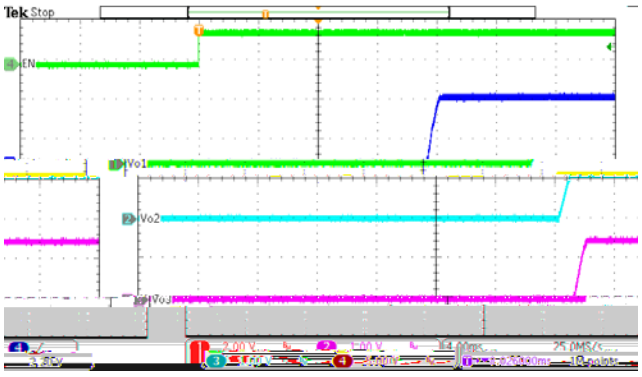

Figure 10. EN On

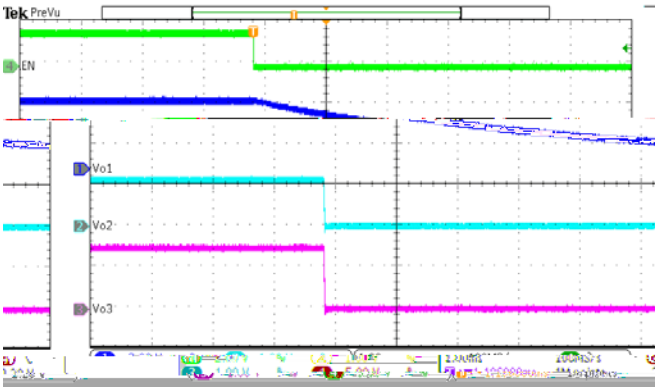

Figure 11. EN Off

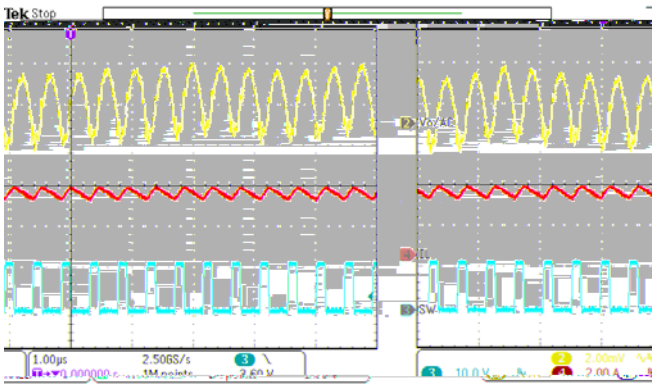

Figure 12. Buck1 Steady State (Io1 = 3A)

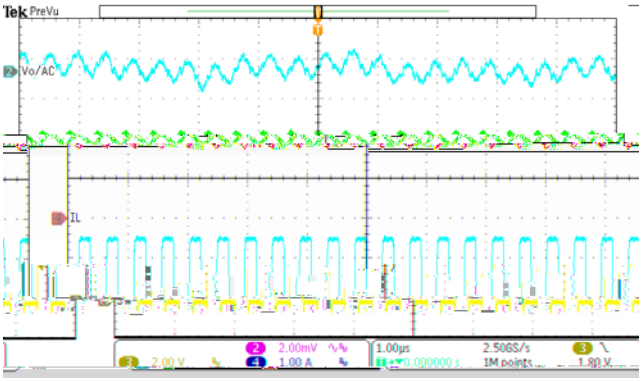

Figure 13. Buck2 Steady State (Io2 = 2A)

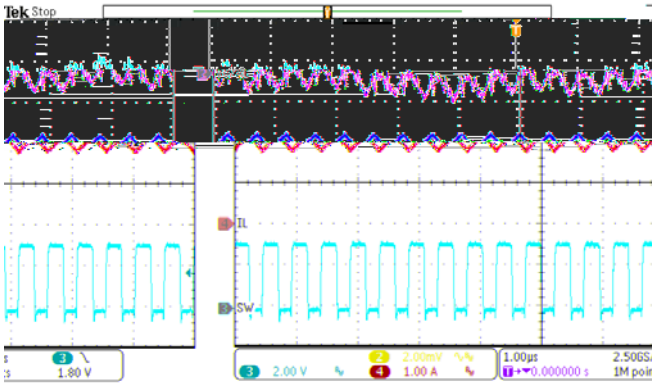

Figure 14. Buck3 Steady State (Io3 = 2A)

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Layout Guideline

Proper PCB layout is a critical for device's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The rule of thumb is to make ground trace lowest impendence and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.

2. Make sure the ground path between VIN capacitor and PGND1 pin is shortest with lowest impendence.

3. Place a low ESR ceramic capacitor as close to VIN1 and VIN23 pin and the ground as possible to reduce parasitic effect.

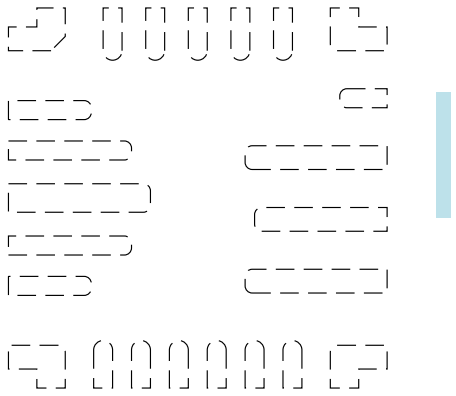
4. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.

5. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias.

6. Output inductor should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.

7. EN UVLO adjust resistors and feedback trace should connect to small signal ground which must return to the GND pin without any interleaving with power ground.

8. For achieving better thermal performance, a four-layer layout is strongly recommended. NCV



LOCK

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CHIPID [7:0]				
ADDRESS: 0x00				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**

				10: Scale=2.5ms. Delay ranges from 0-37.5ms 11: Scale =5ms. Delay ranges from 0-75ms

CONFIG_T2 [7:0]				
ADDRESS: 0x03				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RESERVED	R	/	/
[5]	DF_SCALE	W/R	OV/UV Digital Filter. Adds additional filtering to all OV/UV comparators.	Analog Filter Time = 10µs. Added Digital Filter Time =DF[4:0] x 2µs, when DF_SCALE=0, =DF[4:0] x 10µs, when DF_SCALE=1.
[4:0]	DF	W/R		

CONFIG_EN [7:0]				
ADDRESS: 0x05				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RESERVED	R	/	/
[5]	EN4	W/R	Enable for LDO OUT4. This bit will be activated every time entering DEEPSAFE state, don't change this bit in NORMAL state.	0 = Output Disabled 1 = Output Enabled
[4]	RESERVED	R	/	/
[3]	EN3	W/R	Enable for LV BUCK OUT3. This bit will be activated every time entering DEEPSAFE state, don't change this bit in NORMAL state.	0 = Output Disabled 1 = Output Enabled
[2]	EN2	W/R	Enable for LV BUCK OUT2. This bit will be activated every time entering DEEPSAFE state, don't change this bit in NORMAL state.	0 = Output Disabled 1 = Output Enabled
[1]	RESERVED	R	/	/
[0]	EN_ALL	W/R	Enable for all channel	0 = Output Disabled 1 = Output Enabled

CONFIG_PU1 [7:0]				
ADDRESS: 0x06				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:4]	ON_DELAY4	W/R	OUT4 Power-Up and Recover Turn On delay.	when DELAY_SCALE=00, t_{ON_DELAY4} = ON_DELAY4[3:0] x 0.5ms when DELAY_SCALE=01, t_{ON_DELAY4} = ON_DELAY4[3:0] x 1ms when DELAY_SCALE=10, t_{ON_DELAY4} = ON_DELAY4[3:0] x 2.5ms when DELAY_SCALE=11, t_{ON_DELAY4} = ON_DELAY4[3:0] x 5ms
[3:0]	RESERVED	R	/	/

CONFIG_PU2 [7:0]				
ADDRESS: 0x07				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**

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[7:4]	ON_DELAY3	W/R	OUT3 Power-Up and Recover Turn On delay.	when DELAY_SCALE=00, t_{ON_DELAY3} = ON_DELAY3[3:0] x 0.5ms when DELAY_SCALE=01, t_{ON_DELAY3} = ON_DELAY3[3:0] x 1ms when DELAY_SCALE=10, t_{ON_DELAY3} = ON_DELAY3[3:0] x 2.5ms when DELAY_SCALE=11, t_{ON_DELAY3} = ON_DELAY3[3:0] x 5ms
[3:0]	ON_DELAY2	W/R	OUT2 Power-Up and Recover Turn On delay.	when DELAY_SCALE=00, t_{ON_DELAY2} = ON_DELAY2[3:0] x 0.5ms when DELAY_SCALE=01, t_{ON_DELAY2} = ON_DELAY2[3:0] x 1ms when DELAY_SCALE=10, t_{ON_DELAY2} = ON_DELAY2[3:0] x 2.5ms when DELAY_SCALE=11, t_{ON_DELAY2} = ON_DELAY2[3:0] x 5ms

RSTMAP [7:0]				
ADDRESS: 0x08				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RESERVED	R	/	/
[5]	RSTMAP_VO4	W/R	RESETB Pin Mapping for OUT4.	0 = OV[4] and UV[4] not mapped to RESETB pin 1 = OV[4] and UV[4] are mapped to RESETB pin
[4]	RESERVED	R	/	/
[3]	RSTMAP_VO3	W/R	RESETB Pin Mapping for OUT3.	0 = OV[3] and UV[3] not mapped to RESETB pin 1 = OV[3] and UV[3] are mapped to RESETB pin
[2]	RSTMAP_VO2	W/R	RESETB Pin Mapping for OUT2.	0 = OV[2] and UV[2] not mapped to RESETB pin 1 = OV[2] and UV[2] are mapped to RESETB pin

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[5]	UV_WAR4	Read Clear	UV warning for OUT4, Digital Filter is not included	0 = OUT4 is above UV threshold before DF 1 = OUT4 is below UV threshold before DF
[4]	RESERVED	R	/	/
[3]	UV_WAR3	Read Clear	UV warning for OUT3, Digital Filter is not included	0 = OUT3 is above UV threshold before DF 1 = OUT3 is below UV threshold before DF
[2]	UV_WAR2	Read Clear	UV warning for OUT2, Digital Filter is not included	0 = OUT2 is above UV threshold before DF 1 = OUT2 is below UV threshold before DF
[1]	UV_WAR1	Read Clear	UV warning for OUT1, Digital Filter is not included	0 = OUT1 is above UV threshold before DF 1 = OUT1 is below UV threshold before DF
[0]	RESERVED	R	/	/

STATOV [7:0]				
ADDRESS: 0x0B				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	OV	Read Clear	OV Comparator Status for all channels with Digital Filter.	0 = All enabled channels are below OV threshold after DF 1 = Any enabled channel is above OV threshold after DF
[6]	RESERVED	R	/	/
[5]	OV_WAR4	Read Clear	OV warning for OUT4, Digital Filter is not included	0 = OUT4 is below OV threshold before DF 1 = OUT4 is above OV threshold before DF
[4]	RESERVED	R	/	/
[3]	OV_WAR3	Read Clear	OV warning for OUT3, Digital Filter is not included	0 = OUT3 is below OV threshold before DF 1 = OUT3 is above OV threshold before DF
[2]	OV_WAR2	Read Clear	OV warning for OUT2, Digital Filter is not included	0 = OUT2 is below OV threshold before DF 1 = OUT2 is above OV threshold before DF
[1]	OV_WAR1	Read Clear	OV warning for OUT1, Digital Filter is not included	0 = OUT1 is below OV threshold before DF 1 = OUT1 is above OV threshold before DF
[0]	RESERVED	R	/	/

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[5]	OFF4	Read Clear	OFF Comparator Status for OUT4	0 = OUT4 is above OFF threshold 1 = OUT4 is below OFF threshold
[4]	RESERVED	R	/	/
[3]	OFF3	Read Clear	OFF Comparator Status for OUT3	0 = OUT3 is above OFF threshold 1 = OUT3 is below OFF threshold
[2]	OFF2	Read Clear	OFF Comparator Status for OUT2	0 = OUT2 is above OFF threshold 1 = OUT2 is below OFF threshold
[1]	OFF1	Read Clear	OFF Comparator Status for OUT1	0 = OUT1 is above OFF threshold 1 = OUT1 is below OFF threshold
[0]	RESERVED	R	/	/

STATD [7:0]				
ADDRESS: 0x0D				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	RESERVED	R	/	/
[6]	CLK_ERR	Read Clear	CLK fault indicator	0 = No fault detected 1 = CLK error detected
[5]	SUP_ERR	Read Clear	Supply fault indicator, include VCC OV fault and VIN OV fault	0 = No fault detected 1 = VCC OV or VIN OV detected
[4]	RST_ENTER	Read Clear	RESET state indicator	0 = No fault detected 1 = RESET state has entered since the last read.
[3]	DEEPSAFE_ENTER	Read Clear	DEEPSAFE state indicator	0 = No fault detected 1 = DEEPSAFE state has entered since the last read.
[2]	PIN_ERR	Read Clear	Pin fault indicator, include RESETB Pin stuck fault and GND pin LOSS fault	0 = No fault detected 1 = RESETB Short to supply detected or pull-down fail or GND LOSS since the last read
[1]	THSD	Read Clear	Thermal Shutdown Indication	0 = No thermal shutdown 1 = Thermal shutdown has occurred since last read
[0]	RESERVED	R	/	/

STATWD [7:0]				
ADDRESS: 0x0E				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RESERVED	R	/	/
[5]	RESETB_STAT	R	RESETB Pin State. Allows verification of the state of the RESETB pin. This is the real-time RESETB pin state.	0 = RESETB is low 1 = RESETB is high
[4]	WD_OPEN	R	Watchdog Open Window. This bit indicates that it is permissible to update the watchdog. This bit shows real-time status.	0 = Watchdog update not open 1 = Watchdog ok to update
[3]	WD_ERR	R	Watchdog ERROR for 1 time or 2 times (config by WD_FAIL_CNT), LFSR mismatch is not included	0 = No error detected 1 = Error detected

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[2]	WD_LFSR	Read Clear	LFSR Write Mismatch. The MCU/SoC did not write the correct value to the WDKEY register.	0 = LFSR key match 1 = LFSR key mismatch since last read
[1]	WD_UV	Read Clear	Watchdog Update Violation. The MCU/SoC wrote to the WDKEY register during the CLOSE window.	0 = No violation detected 1 = Watchdog updated too early
[0]	WD_EXP	Read Clear	Watchdog Open Window Expired. The MCU/SoC did not write to the WDKEY register during the whole window.	0 = Watchdog timer not expired 1 = Watchdog timer expired

VOUT2 [7:0]				
ADDRESS: 0x0F				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	RESERVED	R	/	/
[4:0]	OUT2	W/R	OUT2 Voltage Setting	VOUT2 = OUT2[4:0] x 50mV + 0.8V (0.8V to 2.35V)

VOUT3 [7:0]				
ADDRESS: 0x10				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:5]	RESERVED	R	/	/
[4:0]	OUT3	W/R	OUT3 Voltage Setting	VOUT3 = OUT3[4:0] x 50mV + 0.8V (0.8V to 2.35V)

CONFIG_MISC [7:0]				
ADDRESS: 0x11				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	GPIO_SEL	W/R	GPIO pin function, and this bit is invalid when changed online.	00 = Reserved 01 = WDDIS (input) 10 = SYNC (input) 11 = Reserved
[5]	RESERVED	R	/	/
[4]	VIN_OVP_EN	W/R	Enable of VIN OVP. When VIN>43V, part enter DEEPSAFE mode.	0 = Disabled 1 = Enabled
[3:2]	VIN_START	W/R	VIN start threshold at VIN rising	00 = 3.2V; 01 = 4V; 10 = 5V; 11 = 6V
[1:0]	VIN_STOP	W/R	VIN stop threshold at VIN falling	00 = 2.8V; 01 = 3.5V; 10 = 4.5V; 11 = 5.5V

CONFIG_PFM [7:0]				
ADDRESS: 0x12				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:3]	RESERVED	R	/	/
[2]	PFM3	W/R	BUCK3 FCCM/PFM mode selection when NORMAL mode.	0 = FCCM 1 = PFM
[1]	PFM2	W/R	BUCK2 FCCM/PFM mode selection when NORMAL mode.	0 = FCCM 1 = PFM
[0]	PFM1	W/R	BUCK1 FCCM/PFM mode selection when NORMAL mode.	0 = FCCM 1 = PFM

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				If configured as a QA watchdog, writing the incorrect response to the WDKEY register will result in the value written being ignored and a WD_LFSR violation. Writing the correct response in QA mode during an open window will result in a refresh and the WDKEY register being updated. Writing the correct response in QA mode during a closed window will result in the write being ignored and a WD_UV violation. LFSR polynomial: x8 + x6 + x5 + x4 + 1

WD_LOCK [7:0]				
ADDRESS: 0x17				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:1]	RESERVED	R	/	/
[0]	WDLOCK	W/R	Watchdog Lock Protection	0 = Watchdog configuration registers are writeable 1 = Watchdog configuration registers are read-only

CONFIG_PGSEL1 [7:0]				
ADDRESS: 0x19				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	DEEP_OVP_SEL	W/R	Deep OVP threshold selection for all channels.	00 = +15%, others are reserved
[5:4]	DEEP_UVP_SEL	W/R	Deep UVP threshold selection for all channels.	00 = -25%; 01 = -20%; 10 = -15%; 11 = -10%
[3:2]	RESERVED	R	/	/
[1:0]	PG4_SEL	W/R	OUT4 OV/UV threshold selection.	00 = Reserved; 01 = ±6%; 10 = ±8%; 11 = ±10%

CONFIG_PGSEL2 [7:0]				
ADDRESS: 0x1A				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RESERVED	R	/	/
[5:4]	PG3_SEL	W/R	OUT3 OV/UV threshold selection.	00 = Reserved; 01 = ±6%; 10 = ±8%; 11 = ±10%
[3:2]	PG2_SEL	W/R	OUT2 OV/UV threshold selection.	00 = Reserved; 01 = ±6%; 10 = ±8%; 11 = ±10%
[1:0]	PG1_SEL	W/R	OUT1 OV/UV threshold selection.	00 = Reserved; 01 = ±6%; 10 = ±8%; 11 = ±10%

I2C_LOCK [7:0]
ADDRESS: 0x1C

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[0]	I2C_LOCK	W/R	Lock Protection. If 0 by default, then this bit can be changed through the I2C.	0 = All registers can be written. 1 = Writes are ignored to protected registers.

SYS_STATE [7:0]				
ADDRESS: 0x22				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	OTP_CRC_ERR	R	when OTP CRC has error, this bit=1	0 = pass 1 = fail
[6]	RESERVED	R	/	/
[5]	RESERVED	R	/	/
[4]	RESERVED	R	/	/
[3:0]	SYS_STATE	R	System state machine.	0000 = IDLE, 0010 = DEEPSAFE, 0011 = LOADOTP, 0101 = NORMAL, 0111 = POWERUP, 1101 = RESET, others are reserved

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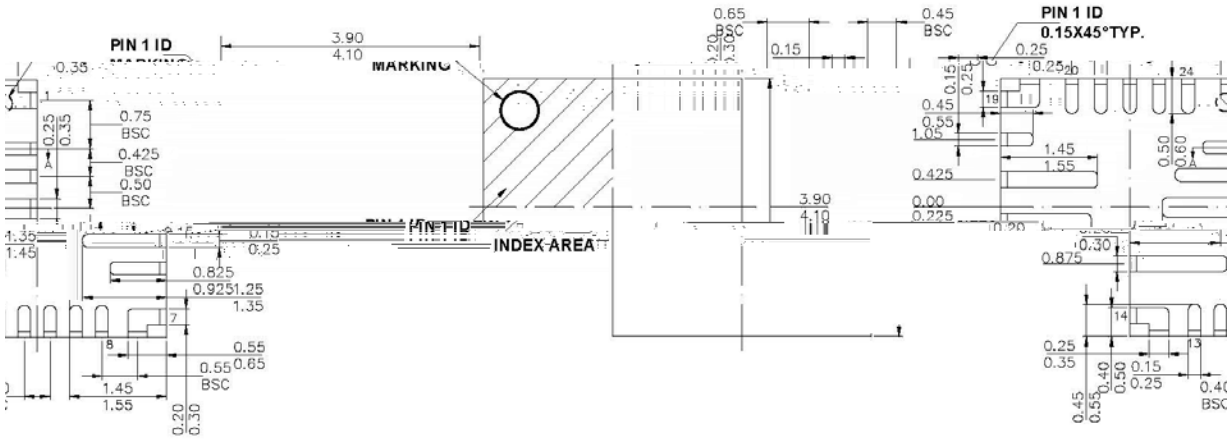

TOM VIEW

TOP VIEW

BOT

SECTION A-A

SIDE VIEW

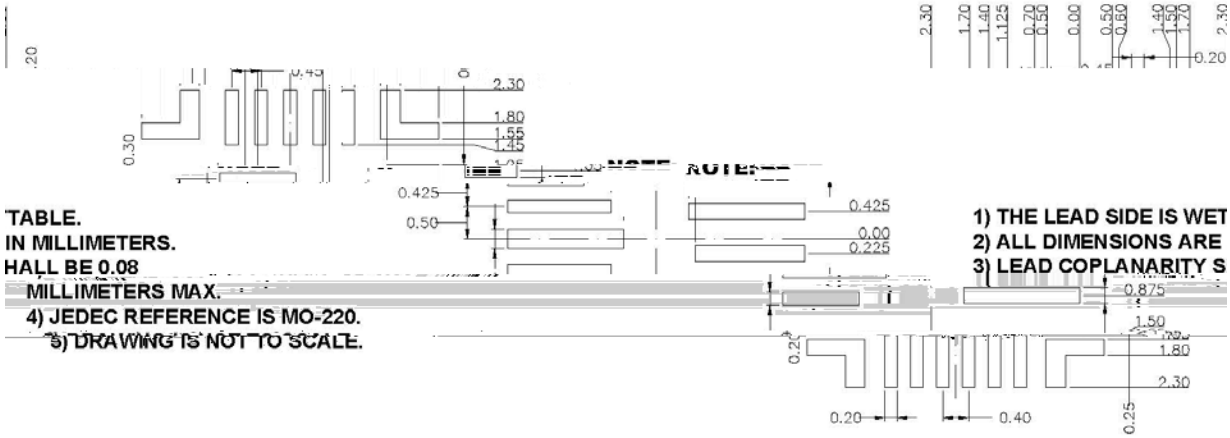

TABLE.
IN MILLIMETERS.
HALL BE 0.08
MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

1) THE LEAD SIDE IS WET
2) ALL DIMENSIONS ARE
3) LEAD COPLANARITY S

RECOMMENDED LAND PATTERN

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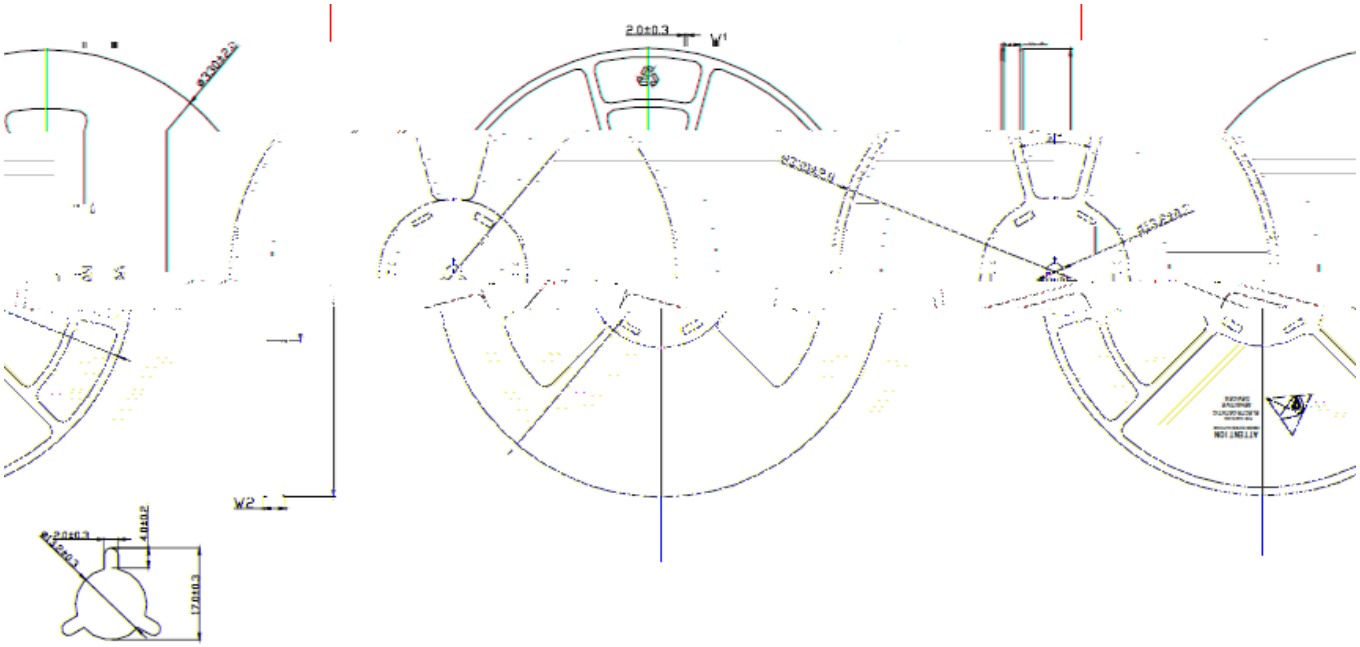

PRODUCT SPECIFICATIONS				
TYPE WIDTH	ØA	ØN	W1 (Min)	W2 (Max)
12MM	330±2.0	100±1.0	12.4	19.4
16mm	330±2.0	100±1.0	16.4	23.4
24MM	330±2.0	100±1.0	24.4	31.4
32MM	330±2.0	100±1.0	32.4	39.4
44MM	330±2.0	100±1.0	44.4	51.4

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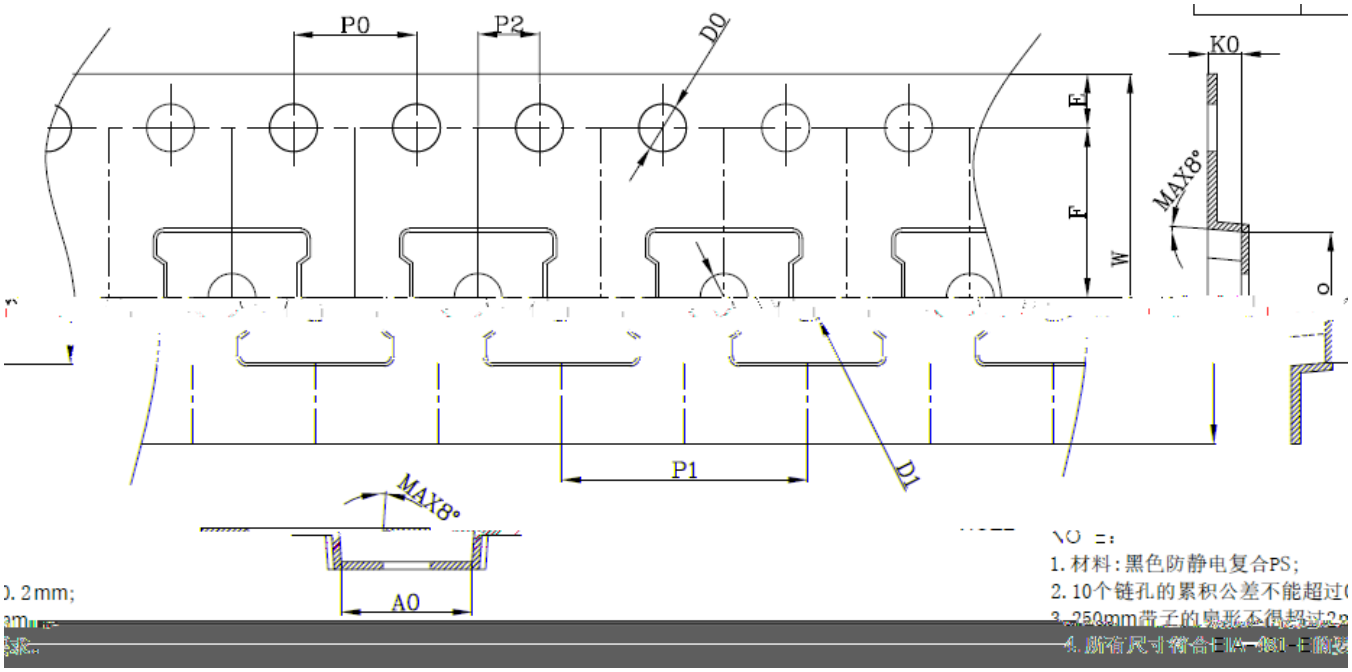

SYMBOL	A0	B0	K0	P0	P1	P2
0±0.10	1.10±0.10	4.00±0.10	8.00±0.10	2.00±0.05	SPEC	4.30±0.10
E	F	D0	D1	W	SYMBOL	T
5±0.10	5.50±0.05	1.55±0.05	1.55±0.10	12.00±0.30	SPEC	0.30±0.05

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