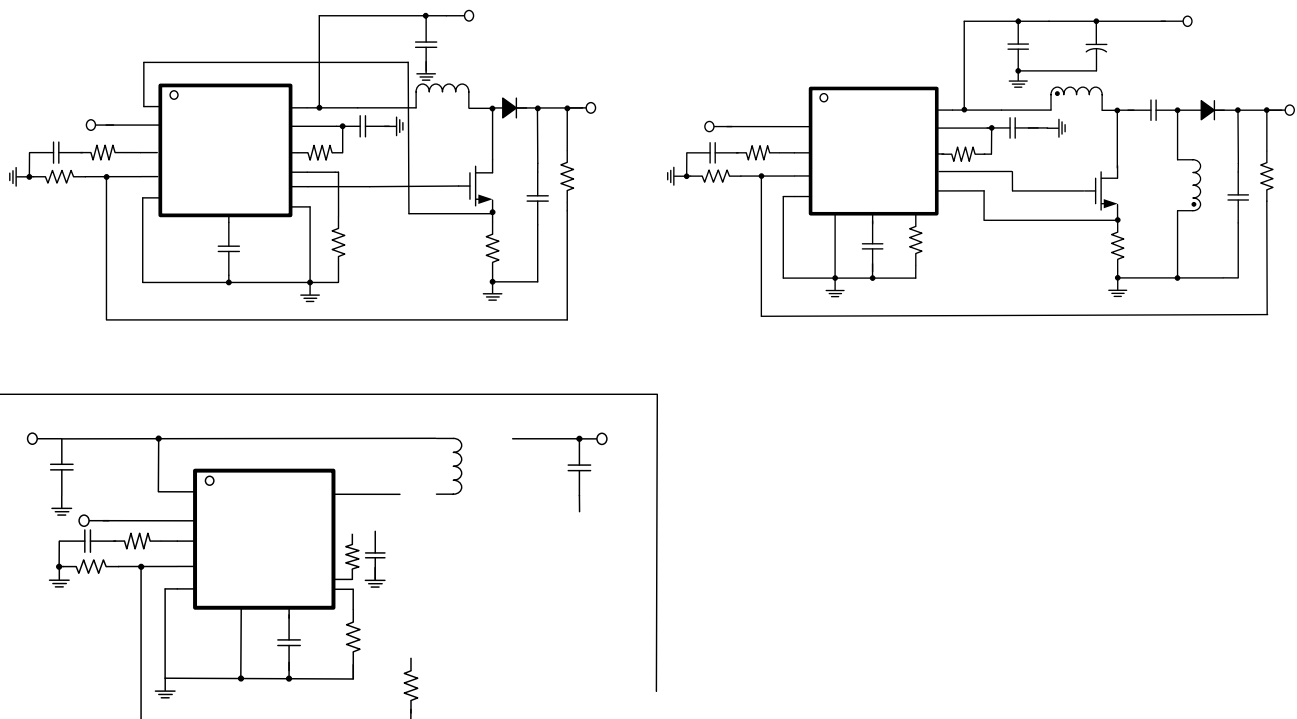


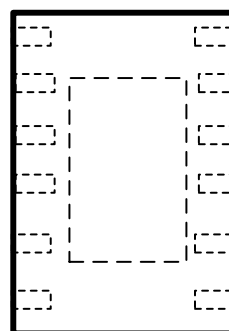


SCT81623Q



ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL

DESCRIPTION	MIN	MAX	UNIT
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Top View: 12-Lead Plastic TQFN 2

SCT81623Q

NAME	NO.	DESCRIPTION

PARAMETER	DEFINITION	MIN	MAX	UNIT

PARAMETER	DEFINITION	MIN	MAX	UNIT

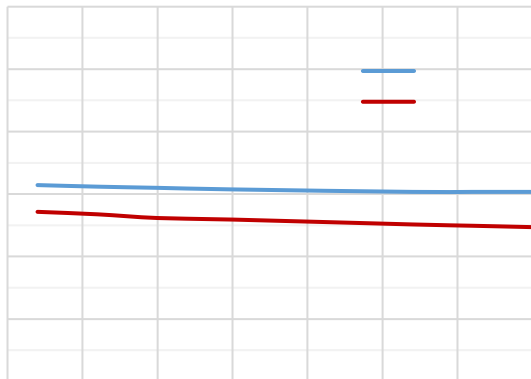
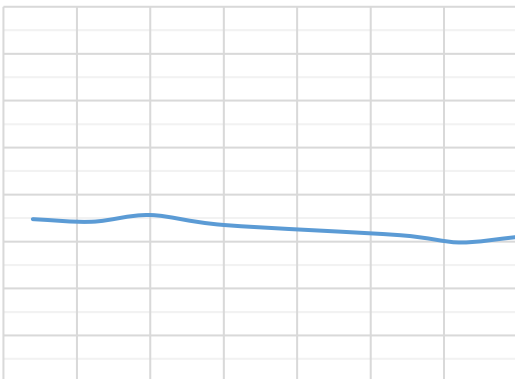
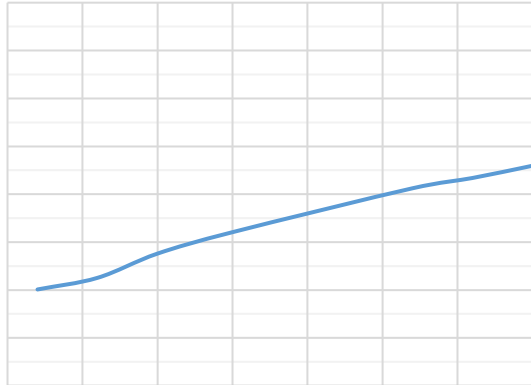
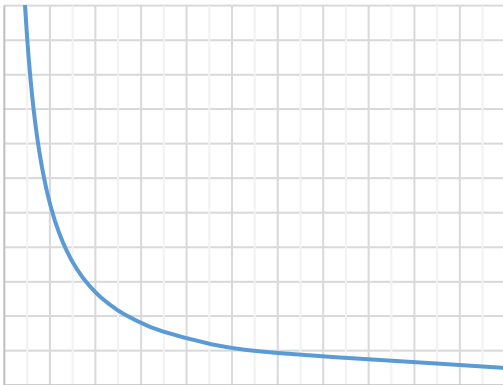
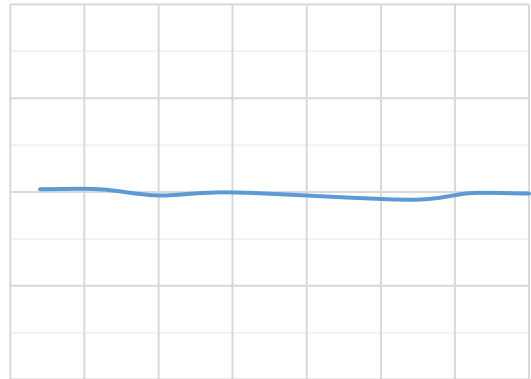
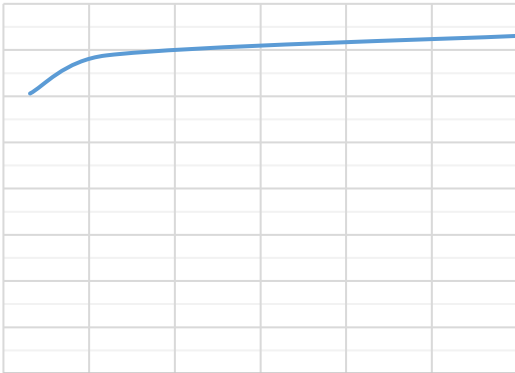
PARAMETER	THERMAL METRIC	TQFN-12L	UNIT

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
VCC Power						
UVLO/EN/SYNC						
Reference and Control Loop						

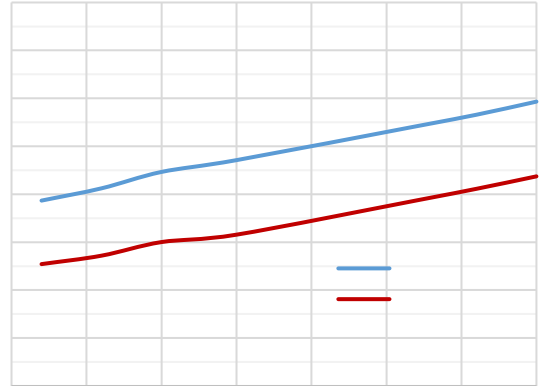
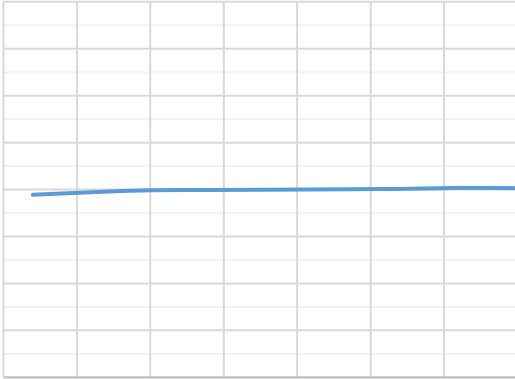
SCT81623Q

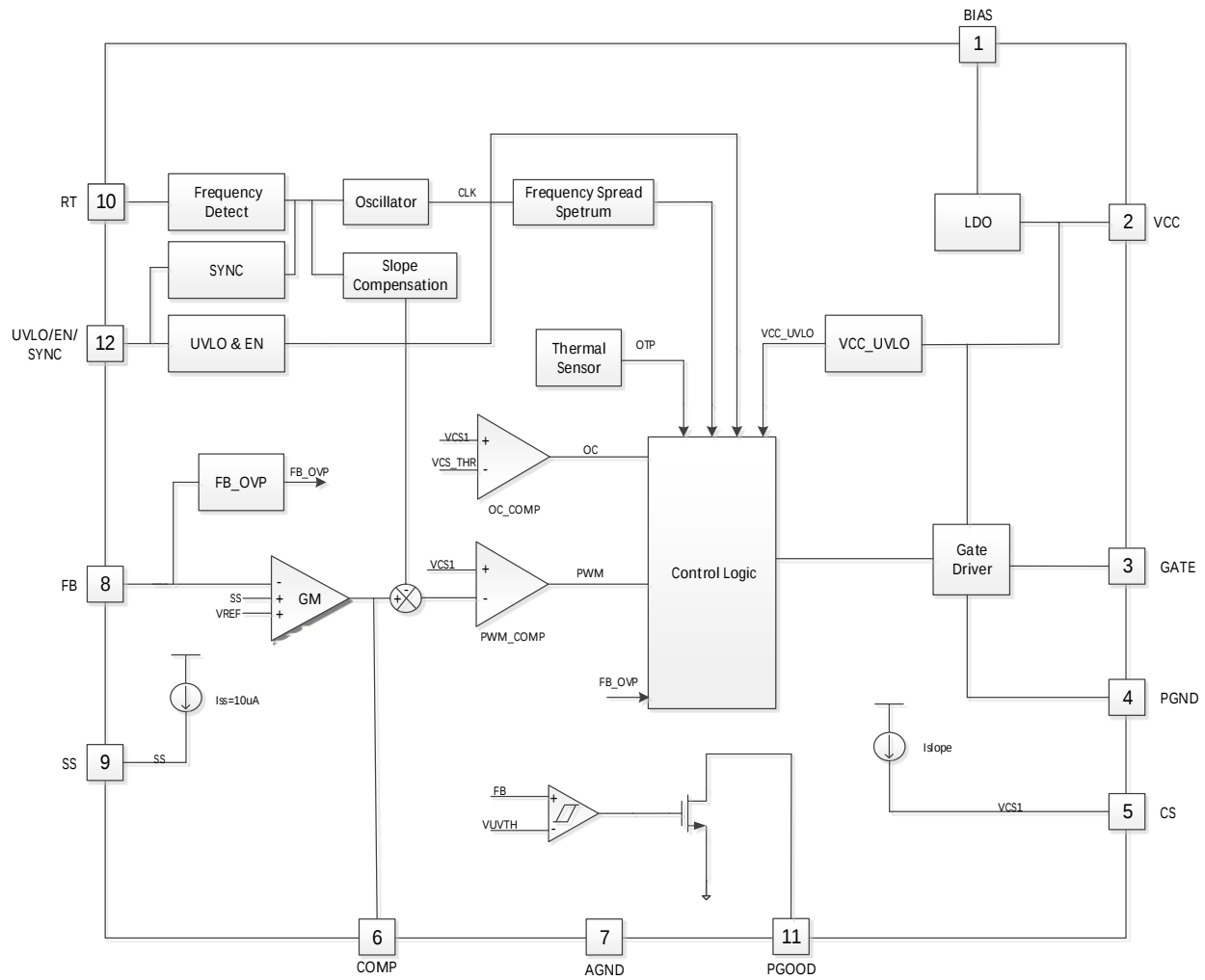
SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Current Sense						

u



11

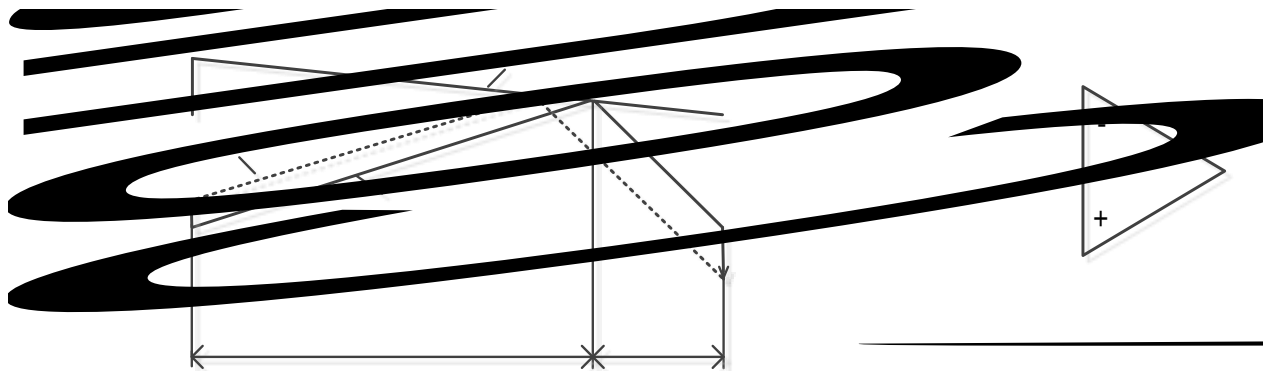




Overview

Overvoltage Protection

Slope Compensation Ramp



:

$$H \qquad \ast D_{E @}$$

:

$$_1 \qquad \ast D_{E @}$$

$$_2 \qquad \ast D_{E @}$$

$$_1 \qquad \ast D_{E @} \quad H \quad \ast D_{E @} /$$

$$_2 \qquad \ast D_{E @} \quad (H \quad H) \ast D_{E @} /$$

$$H \quad _1 \quad \left(\frac{2}{1} \right) \ast \quad H \quad _0$$

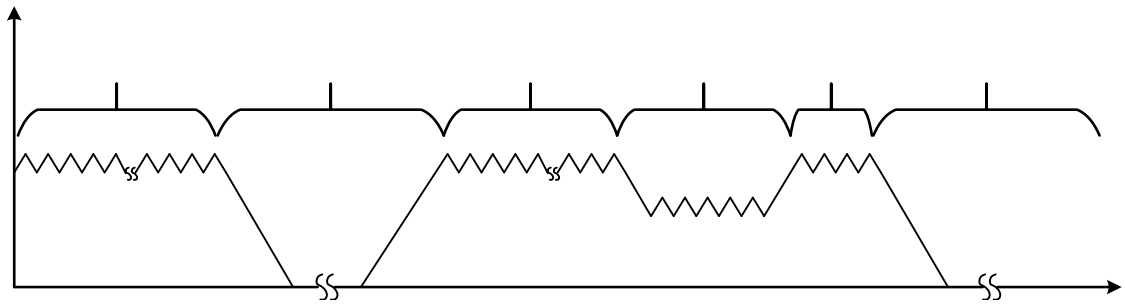
$$H \quad _1 \quad \left(\frac{2}{1} \right) \ast \quad H \quad _0 \quad \left(\frac{}{1} \right) \ast \quad H \quad _0$$

$$\left| \left(\frac{2}{1} \right) \right| \quad 1$$

$$H_E \ast$$

$$(H_E \quad = \ast D_E) \ast$$

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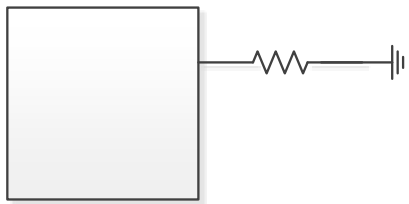


Output Voltage

$$D_F = \frac{H_{AGF} H_b}{H_b} D$$

Switching Frequency

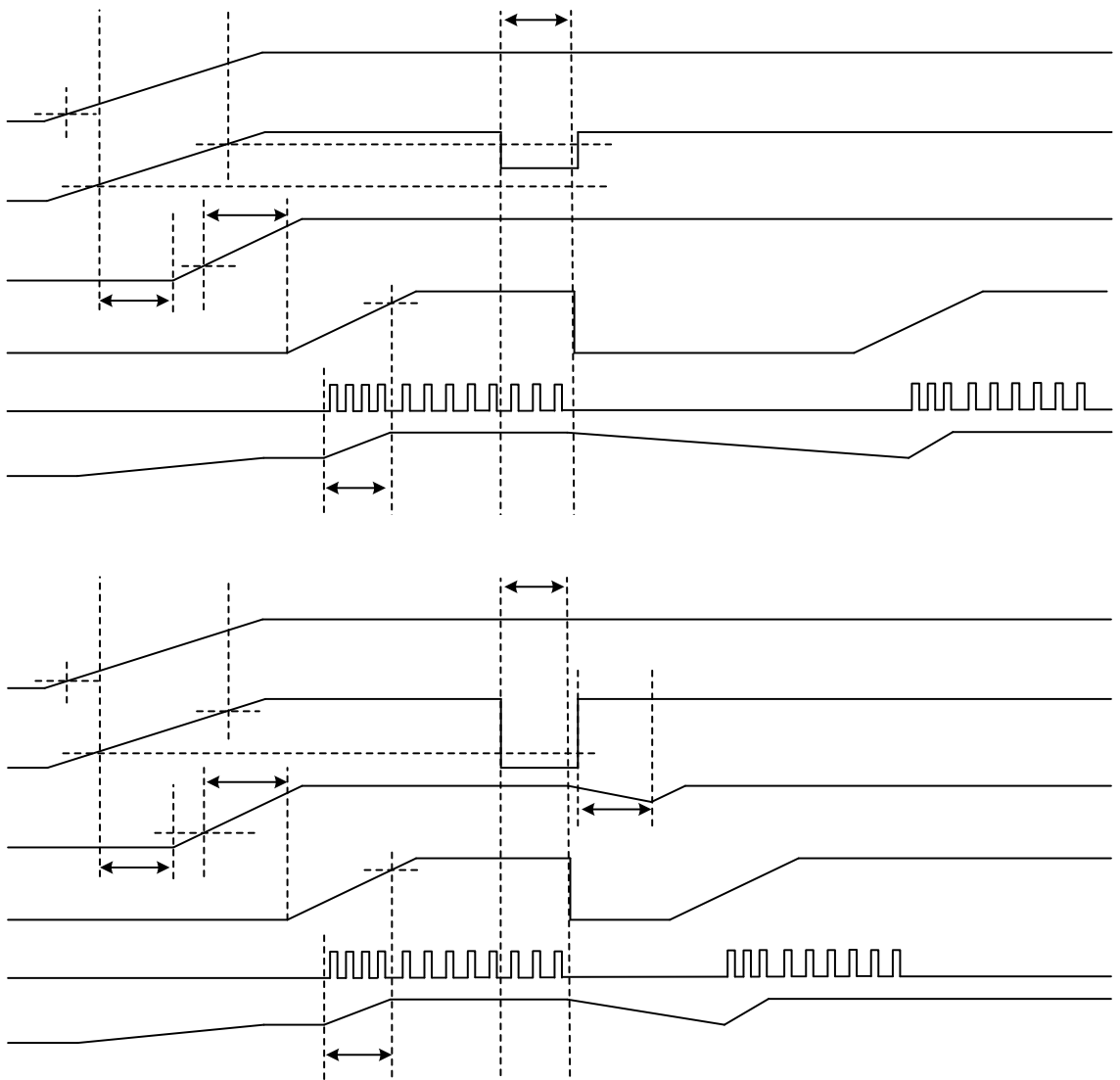
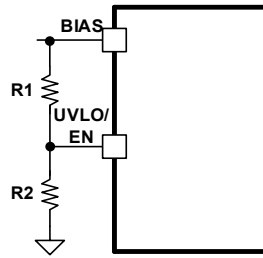
$$D_{DF} = \frac{H_{AGF} H_b}{H_b} D$$



Enable and Under Voltage Lockout

$$D1 = \frac{H_{@_A@} H_{@_A}}{GH_A}$$

$$D2 = D1 * \frac{H_{GH_A @}}{H_{@_A@} H_{GH_A @}}$$



Clock Synchronization

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Frequency Spread Spectrum

Power Good

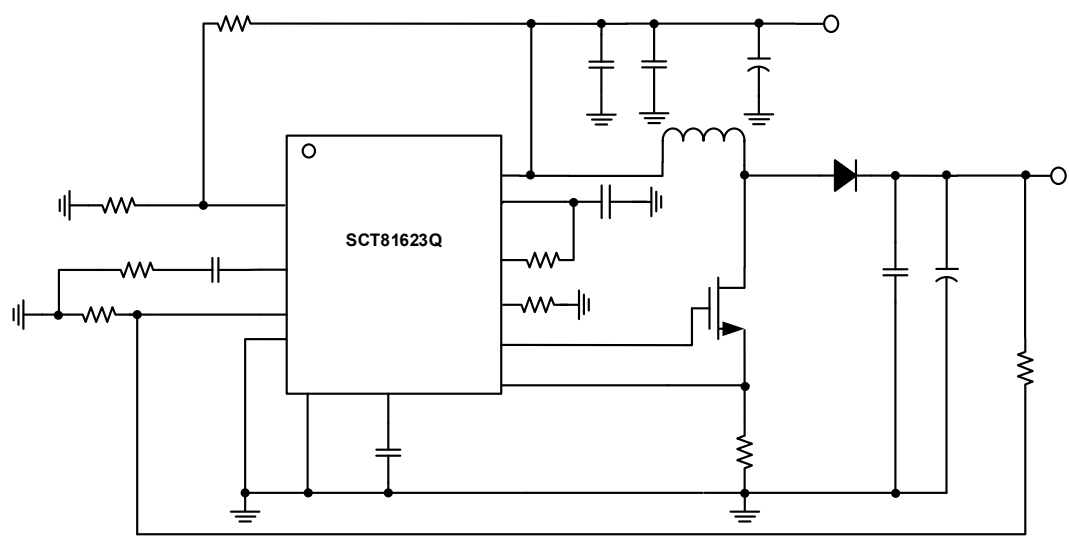
Thermal Shutdown

Shutdown Mode

Standby Mode

Run Mode

Typical Application (Boost)



Design Parameters

Design Parameters	Example Value

Inductor Selection (Boost)

$$5 \frac{H_{AGF} \quad AGF}{H_{@}}$$

$$BB \frac{1}{\frac{1}{H_{AGF} \quad H_{@}} \quad \frac{1}{H_{@}}} EI$$

$$B = 5 \frac{BB}{2}$$

Input Capacitor Selection

$$5 @ (D \quad E) \frac{(H_{AGF} \quad H_{@}) \quad H_{@}}{\sqrt{12} \quad H_{AGF}}$$

Output Capacitor Selection

$$H_{-5} = \frac{(H_{AGF} H_{@-@})_{AGF}}{H_{AGF} 5_{AGF}}$$

$$H_{-ED} B = ED$$

Power MOSFET Selection

$$C_B = B =$$

$$C_{DE} = \sqrt{\left(s^2 \frac{BB}{12} \right)^*}$$

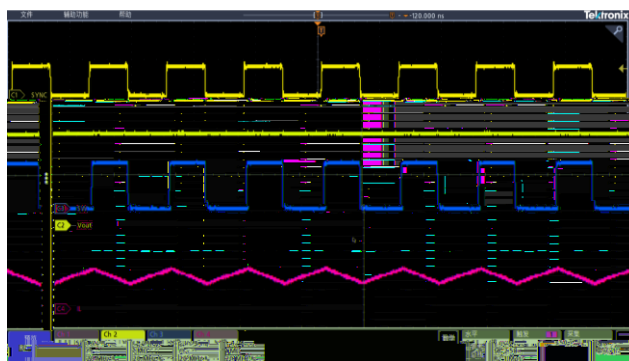
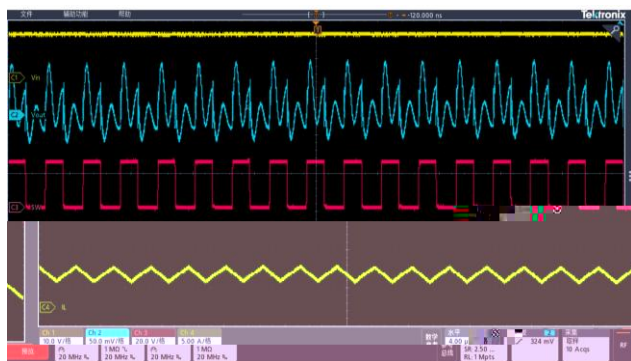
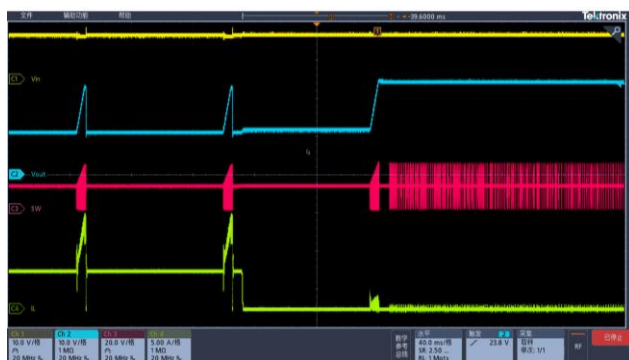
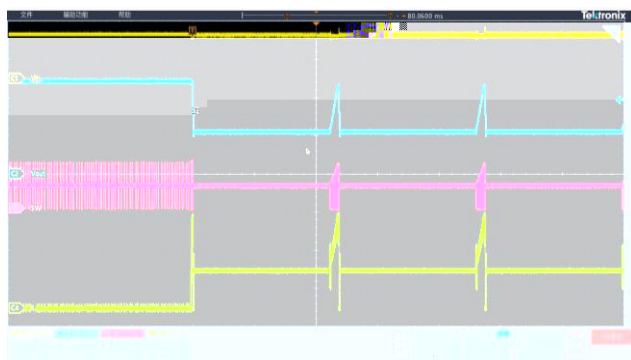
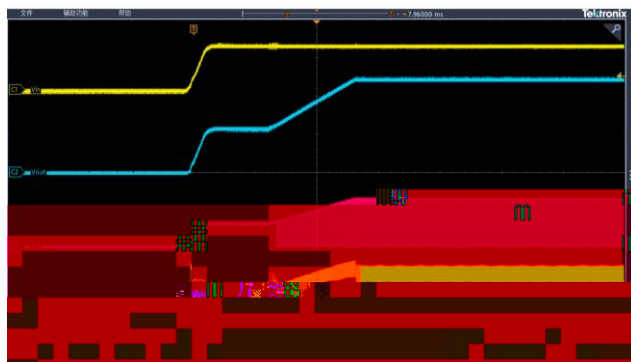
$$B_E = \frac{2}{C_{DE}} D_{E-A@} H_A H_{@-@} C_B = \frac{C}{EI}$$

9

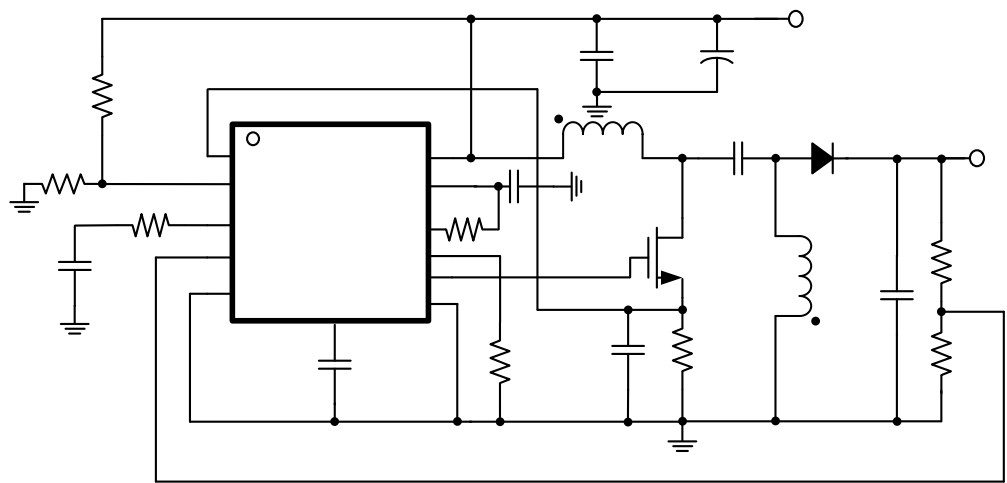
/

Output Diode Selection

Application Waveforms



Typical Application(Sepic)



Design Parameters

Design Parameters	Example Value

Inductor Selection (Sepic)

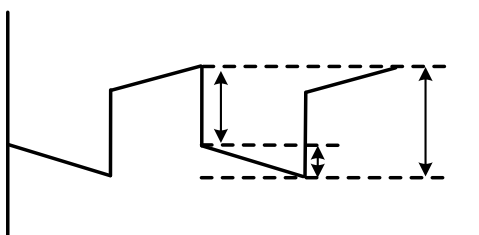
$$\begin{aligned}
 L_1 @ 40\% &= \frac{H_A}{H_{@} @} 40\% \\
 L_2 A 40\% &= \frac{H_A}{H_{@} @} 40\% \\
 L_1 L_2 &= \frac{H_{@} @}{EI} \\
 f \\
 L_{1_B} &= \frac{H_A}{H_{@} @} (1 - \frac{40\%}{2}) \\
 L_{2_B} &= \frac{H_A}{H_{@} @} (1 - \frac{40\%}{2}) \\
 L_1 L_2 &= \frac{H_{@} @}{EI}
 \end{aligned}$$

Power MOSFET Selection

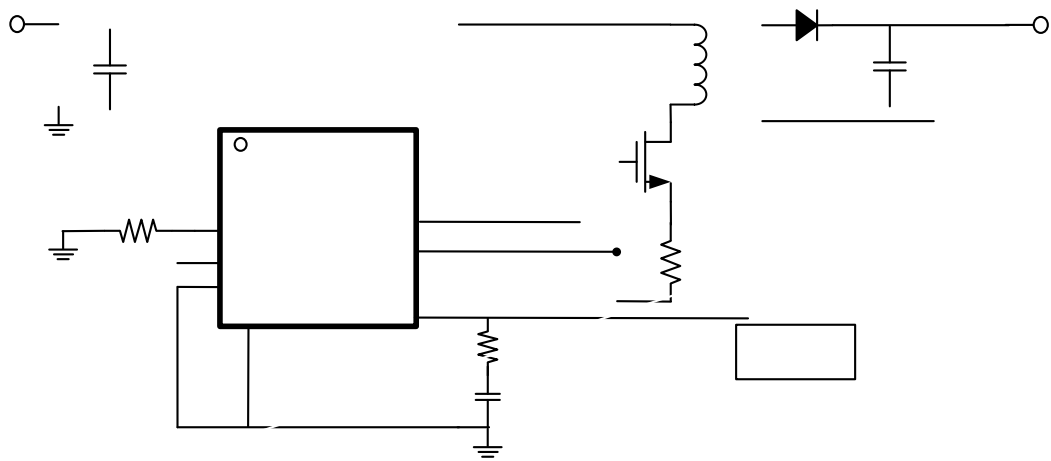
$$\begin{aligned}
 H_{EI_B} &= H_{@} H_A H \\
 C_{B_} &= L_{1_B} = L_{2_B} = \\
 C_{D_E} A &= \sqrt{\frac{H_A H_{@} @ H H_A H}{H_{@} @^2}}
 \end{aligned}$$

Output Diode Selection

$$H_{_B} = H_{@_} H_{_A_}$$



Typical Application(Flyback)



Design Parameters

Design Parameters	Example Value

Transformer Selection (Flyback)

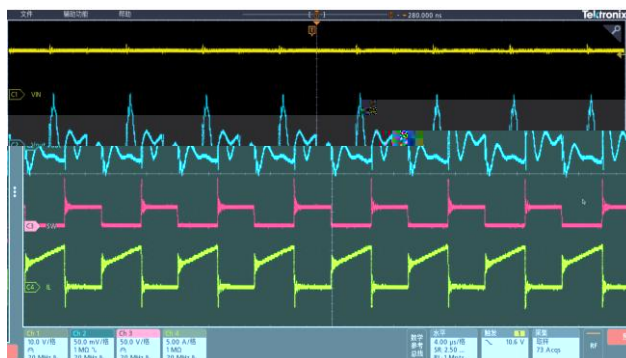
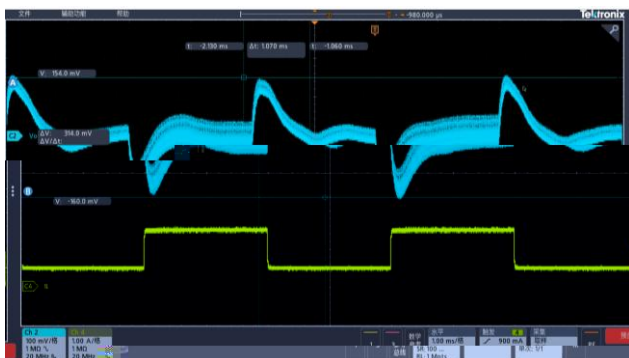
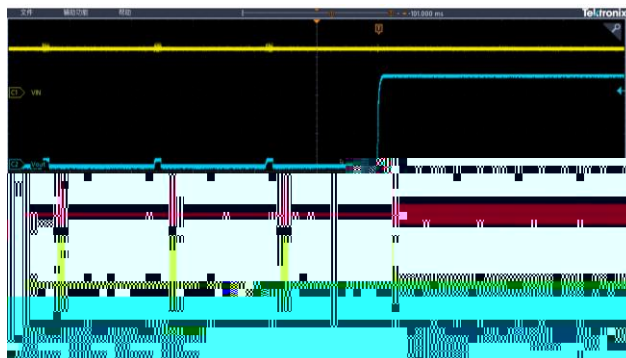
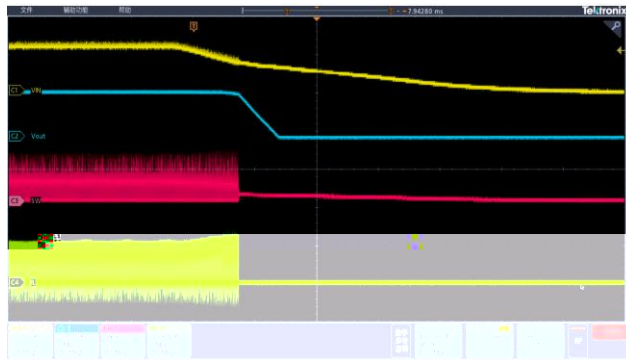
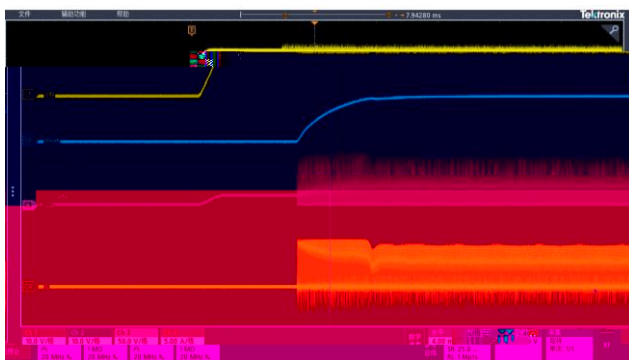
$$\frac{\frac{a_B}{a_E} H_A}{H_{a-} \quad a \quad \frac{a_B}{a_E} H_A}$$

Input Capacitor Selection

$$5 @ \frac{\frac{B_A}{H_{@-@}}}{EI} \frac{1}{H_{EGBB K}}$$

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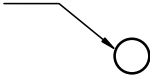
Application Waveforms



Layout Guideline

OUT

PIN 1 ID
MARKING



PIN 1 ID
INDEX AREA



TOP VIEW

PIN 1 ID
0.25X45°TYP.



BOTTOM VIEW

SIDE VIEW

SECTION A-A

NOTE:

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 4) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
- 5) JEDEC REFERENCE IS MO-220.
- 6) DRAWING IS NOT TO SCALE.

RECOMMENDED LAND PATTERN

