NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to production.

Over operating free-air temperature range unless otherwise noted.

V_{IN}	Input voltage range	4.6	28	V
V_{OUT}	Output voltage range	0.6	20	V
T_J	Operating junction temperature	-40	125	°C

V_{ESD}	Human Body Model (HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins	- 2.5	2.5	kV
	Charged Device Model (CDM), per ANSI-JEDEC-JS-002-2014specification, all pins	- 2	2	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

$R_{\theta JA}$ (1)(2)	Junction to ambient thermal resistance	91.86	°C/W
Ψ_{JT} (2)	Junction-to-top characterization parameter	12.73	
Ψ_{JB} (2)	Junction-to-board characterization parameter	24.25	
$R_{\theta JCtop}$ (1)(2)	Junction to case thermal resistance	103.16	
$R_{\theta JB}$ (2)	Junction-to-board thermal resistance	24.5	
$R_{\theta JA\_EVM}$ (3)	Junction to ambient thermal resistance (EVM)	65.61	
Ψ_{JT_EVM} (3)	Junction-to-top characterization parameter (EVM)	8.83	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT233-ch thị M

V_{IN}=12V, T_J=-40°C~125°C, typical value is tested under 25°C.

V_{IN}	Operating input voltage		4.6	28	V
V_{IN_UVLO}	Input UVLO	V_{IN} rising	4.3	4.6	V
	Hysteresis		300		mV
I_{SD}	Shutdown current	EN=0, No load, VIN=12V	1.5	5	

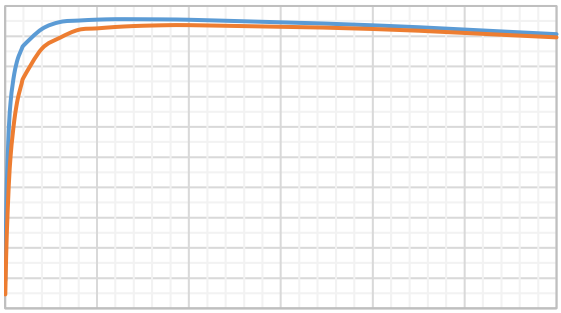


Figure 1. Efficiency vs Load Current, Vout=5V

Figure 2. Efficiency vs Load Current, Vout=12V

Figure 3. Load Regulation, Vin=12V, Vout=5V

Figure 4. Current Limit VS Temperature

Figure 5. Line Regulation, Iout=1A

Figure 6. Reference voltage VS Temperature

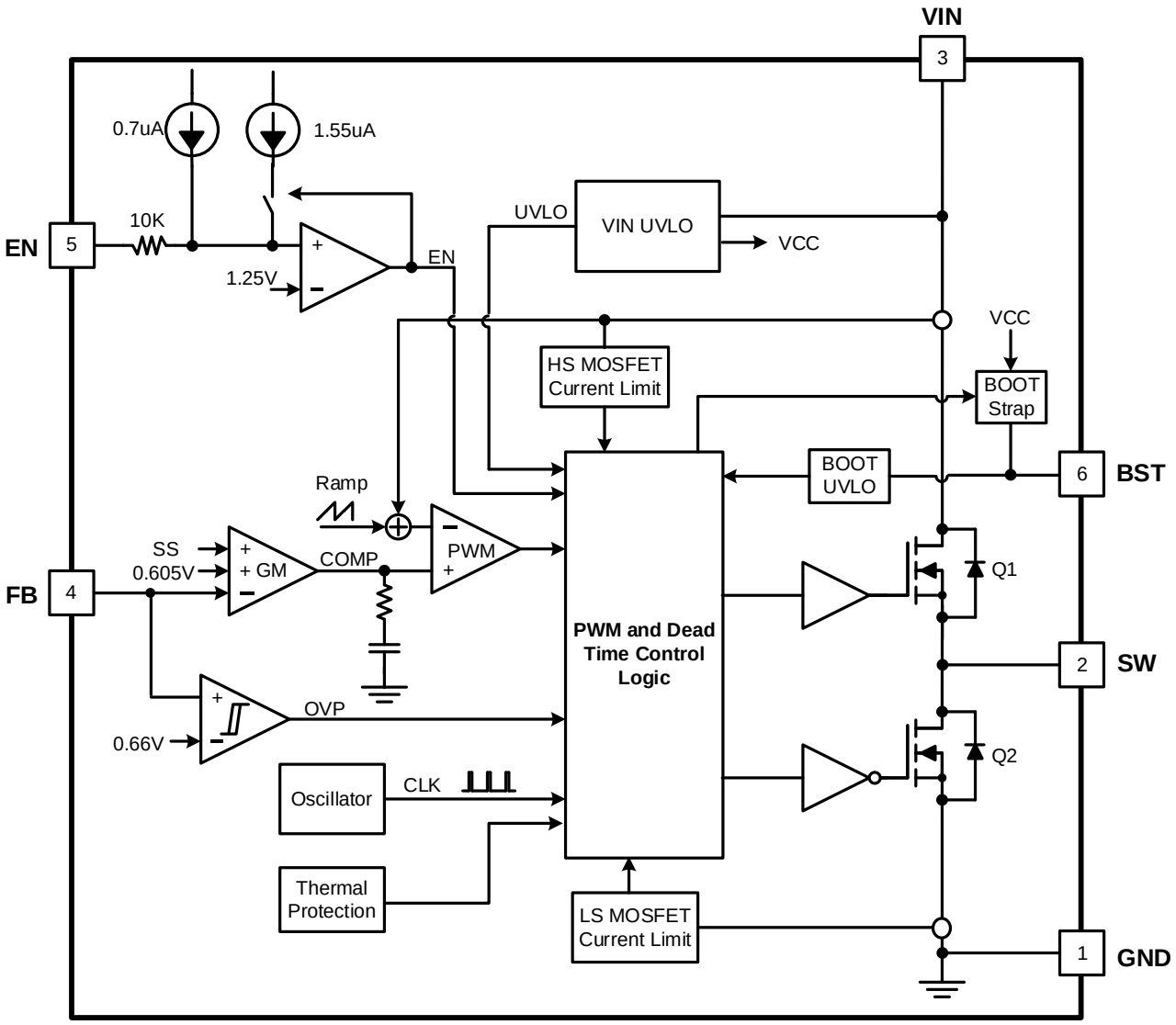


Figure7. Functional Block Diagram

The SCT2331D device is 4.6V-28V input, 3A output, EMI friendly, fully integrated synchronous buck converters. The device employs fixed frequency peak current mode control. An internal clock with 410kHz frequency initiates turning on the integrated high-side power MOSFET Q1 in each cycle, then inductor current rises linearly and the converter charges output cap. When sensed voltage on high-side MOSFET peak current rising above the voltage of internal COMP (see functional block diagram), the device turns off high-side MOSFET Q1 and turns on low-side MOSFET Q2. The inductor current decreases when MOSFET Q2 is ON. In the next rising edge of clock cycle, the low-side MOSFET Q2 turns off. This repeats on cycle-by-cycle based.

The peak current mode control with the internal loop compensation network and the built-in 3ms soft-start simplify the SCT2331D footprints and minimize the off-chip component counts.

The error amplifier serves the COMP node by comparing the voltage on the FB pin with an internal 0.605V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

The quiescent current of SCT2331D is 230uA typical under no-load condition and no switching. When disabling the device, the supply shut down current is only 1.5μA. The SCT2331D works at Forced PWM mode to achieve low ripple in light load condition.

The SCT2331D implements the Frequency Spread Spectrum (FSS) modulation spreading of ±6% centered 410kHz switching frequency. FSS improves EMI performance by not allowing emitted energy to stay in any one receiver band for a significant length of time. The converter has optimized gate driver scheme to achieve switching node voltage ringing-free without sacrificing the MOSFET switching time to further damping high frequency radiation EMI noise.

The hiccup mode minimizes power dissipation during prolonged output overcurrent or short conditions. The hiccup wait time is 16 cycles and the hiccup restart time is 40ms. The SCT2331D device also features protections including cycle-by-cycle high-side MOSFET peak current limit, over-voltage protection, and over-temperature protection.

The SCT2331D is designed to operate from an input voltage supply range between 4.6V to 28V, at least 0.1uF decoupling ceramic cap is recommended to bypass the supply noise. If the input supply locates more than a few inches from the converter, an additional electrolytic or tantalum bulk capacitor or with recommended 22uF may be required in addition to the local ceramic bypass capacitors.

The SCT2331D Under Voltage Lock Out (UVLO) default startup threshold is typical 4.3V with VIN rising and shutdown threshold is 4V with VIN falling. The more accurate UVLO threshold can be programmed through the precision enable threshold of EN pin.

When applying a voltage higher than the EN high threshold (typical 1.25V/rise), the SCT2331D enables all functions and the device starts soft-start phase. The SCT2331D has the built in 3ms soft-start time to prevent the output overshoot and inrush current. When EN pin is pulled low, the internal SS net will be discharged to ground. Buck operation is disabled when EN voltage falls below its lower threshold (typically 1.23V/fall).

An internal 0.7uA pull up current source connected from internal LDO power rail to EN pin guarantees that floating EN pin automatically enables the device. For the application requiring higher VIN UVLO voltage than the default setup, there is a 1.55uA hysteresis pull up current source on EN pin which configures the VIN UVLO voltage with an off-chip resistor divider R3 and R4, shown in Figure 8. The resistor divider R3 and R4 are calculated by equation (1) and (2).

EN pin is a high voltage pin and can be directly connected to VIN to automatically start up the device with VIN rising to its internal UVLO threshold.

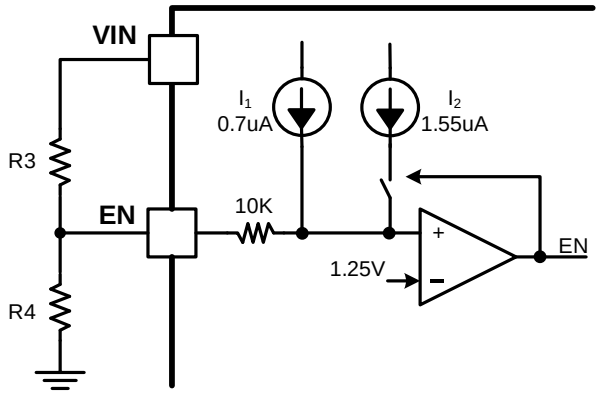


Figure 8. Adjustable VIN UVLO

$$\frac{\overline{\quad}}{\overline{\quad}} \qquad (1)$$

$$\overline{\quad} \qquad (2)$$

Where:

Vstart: Vin rise threshold to enable the device
Vstop: Vin fall threshold to disable the device
I_1=0.7uA
I_2=1.55uA
V_{ENR}=1.25V
V_{ENF}=1.23V

To improve EMI performance, SCT2331D adopts Frequency Spread Spectrum (FSS) to spread the switching noise over a wider band and therefore reduces conducted and radiated interference peak amplitude at particular frequency. The SCT2331D features 410kHz switching frequency with spreading frequency of +/-6% and modulation rate 1/512 of switching frequency. The FSS technique effectively decreases the EMI noise by spreading the switching frequency. As a result, the harmonic wave amplitude is reduced, and the harmonic wave band is wider.

In buck converter, the switching node ringing amplitude and cycles are critical especially related to the high frequency radiation EMI noise. The SCT2331D implements the multi-level gate driver speed technique to achieve the switching node ringing-free without scarifying the switching node rise/fall slew rate and power efficiency of the

converter. The switching node ringing amplitude and cycles are damped by the built-in MOSFETs gate driving technique (SCT Patented Proprietary Design).

The inductor current is monitored during high-side MOSFET Q1 and low-side MOSFET Q2 on. The SCT2331D implements over current protection with cycle-by-cycle limiting high-side MOSFET peak current and low-side MOSFET valley current to avoid inductor current running away during unexpected overload or output hard short condition.

When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The internal COMP voltage ramps up to high clamp voltage. When COMP voltage is clamped for 16 switching cycles, the converter stops switching. After remaining OFF for 40ms the device restarts from soft starting phase. If overload or hard short condition still exists during soft-start and make COMP voltage clamped at high, after soft start time and COMP keep high for 16 switching cycles, the device enters turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating operation.

The hiccup protection mode above makes the average short circuit current to alleviate thermal issues and protect the regulator.

SCT2331D features buck converter output over voltage protection (OVP). If the output feedback pin voltage exceeds 110% of feedback reference voltage (0.605V), the converter stops switching immediately. When the output feedback pin voltage drops below 105% of feedback reference voltage, the converter resumes to switching. The OVP function prevents the connected output circuitry damaged from un-predictive overvoltage. Featured feedback overvoltage protection also prevents dynamic voltage spike to damage the circuitry at load during fast loading transient.

The high-side MOSFET Q1 has minimum on-time 90ns typical limitation. While the device operates at minimum on-time, further increasing VIN results in pushing output voltage beyond regulation point. With output feedback over voltage protection, the converter skips pulse by turning off high-side MOSFET Q1 and prevents output running away higher to damage the load.

An external bootstrap capacitor between BST and SW pin powers floating high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on.

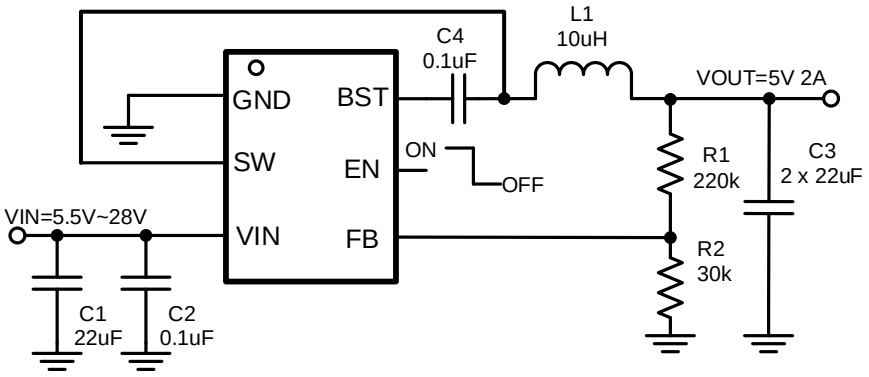
The floating supply (BST to SW) UVLO threshold is 2.65V rising and hysteresis of 250mV. When the converter operates with high duty cycle or prolongs in sleep mode for certain long time, the required time interval to recharging bootstrap capacitor is too long to keep the voltage at bootstrap capacitor sufficient. When the voltage across bootstrap capacitor drops below 2.4V, BST UVLO occurs. The SCT2331D intervenes to turn on low side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee operation over a wide duty range.

To support the application of small voltage-difference between Vout and Vin, the Low Drop Out (LDO) Operation is implemented by the SCT2331D. When VIN is close to output voltage and minimum off time is triggered, switching on time will be extended to avoid output voltage drops, switching frequency will decrease accordingly. After maximum On-time is triggered, SW will be in max duty cycle operation. Thus, the effective duty cycle of the switching regulator during Low Drop-out LDO operation can be very high.

During ultra-low voltage difference of input and output voltages, i.e., the input voltage ramping down to power down, the output can track input closely thanks to LDO operation mode.

The minimum operating frequency limit of about 85kHz can also effectively prevent audio noise interference caused by switching frequency when working with large duty cycle

Once the junction temperature in the SCT2331D exceeds 160°C, the thermal sensing circuit stops converter switching and restarts with the junction temperature falling below 135°C. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.



Design Parameters	Example Value
Input Voltage	12V typical, 5.5~28V
Output Voltage	5V
Output Current	3A
Output voltage ripple (peak to peak)	8mV
Switching Frequency	410kHz

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 5.3A. The most conservative approach is to choose an inductor with a saturation current rating greater than 5.3A. Because of the maximum ILPEAK limited by device, the maximum output current that the SCT2331D can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation (6) desired.

(6)

Where:

Δ is the output voltage ripple.
f_{SW} is the switching frequency.
L is the inductance of inductor.
C_{OUT} is the output capacitance.
V_{OUT} is the output voltage.
V_{IN} is the input voltage.

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 22μF ceramic output capacitors work for most applications.

The SCT2331D features external programmable output voltage by using a resistor divider network R1 and R2 as shown in the typical application circuit Figure10. Use equation (7) to calculate the resistor divider values.

(7)

Set the resistor R2 value to be approximately 30k. Slightly increasing or decreasing R1 can result in closer output voltage matching when using standard value resistors.

V_{IN}=12V, V_{OUT}=5V, unless otherwise noted

Figure 10. Power up (I_{LOAD}=3A)

Figure 11. Power down (I

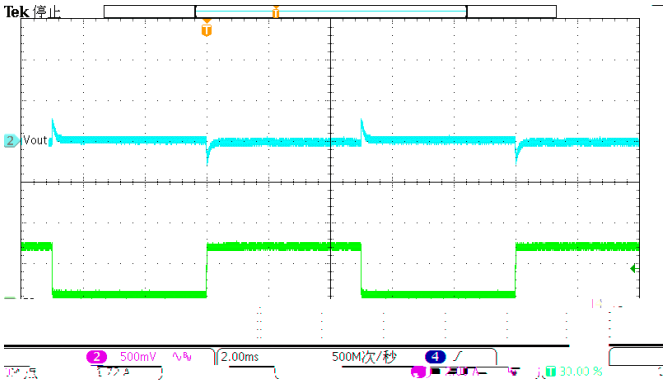


Figure 16. Load Transient (0.3A~2.7A, 1.6A/us)

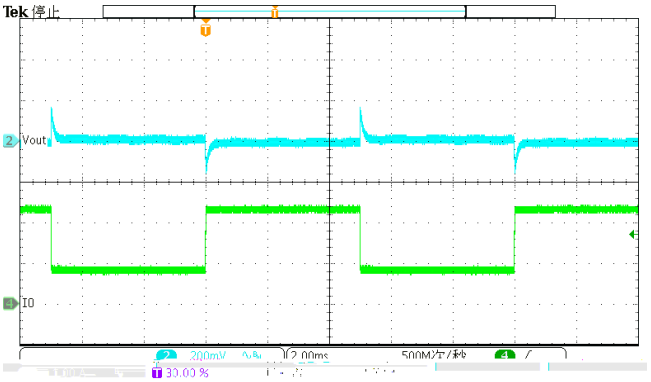


Figure 17. Load Transient (0.75A~2.25A, 1.6A/us)

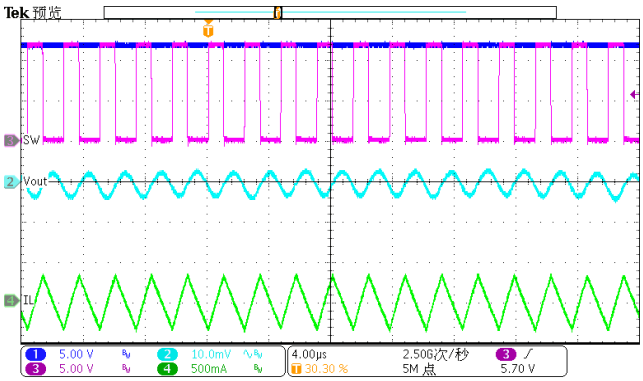


Figure 18. Output Ripple (I_{LOAD}=0A)

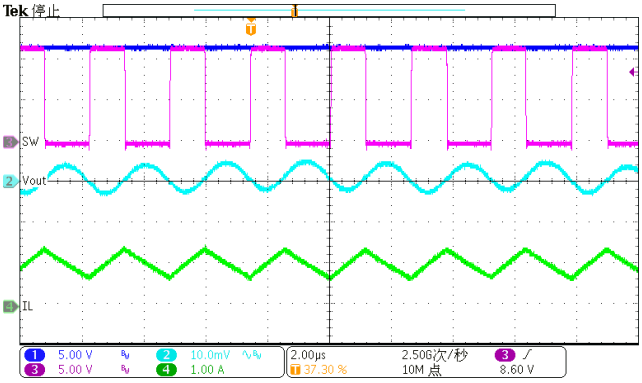


Figure 19. Output Ripple (I_{LOAD}=1A)

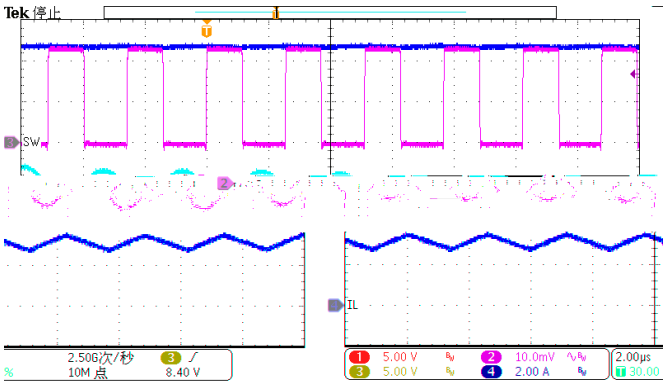
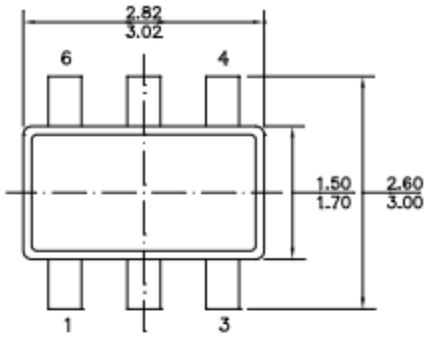
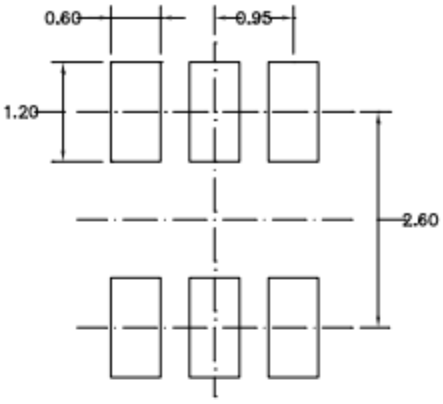


Figure 20. Output Ripple (I_{LOAD}=3A)

Figure 21. Thermal, 12V_{IN}, 5V_{OUT}, 3A



TOP VIEW



RECOMMENDED LAND PATTERN