) HLI DL LF H F

REVISION HISTORY

127(3DJH EH I H L H LL D GWH I DJH EH L KHF H H L

5H LL 5HHD H G F L .

DEVICE ORDER INFORMATION

Orderable Device	Output Voltage	Package	Package Marking	PINS	MSL	Transport Media, Quantity
6&7 07(5	G	(0623 /				7D H 5HH

PIN CONFIGURATION

RECOMMENDED OPERATING CONDITIONS

2 H HDLJIHHDL H HD H D JH H KH LH HG

PARAMETER	DEFINITION	MIN	MAX	UNIT
9,1	, DJH D JH			9
9287	2 DJH D JH			9
9(1	(DEHL DJH		9,1	9
93	3 H J G L DJH			9
(/ <	3 JD DEH3 H G HD 7L H			9
&,1	, FD DFL			)
&287	2 FD DFL			)
(65	2 FD DFL (65 H LH H			
7-	2 HDLJ FL H HD H			&

ABSOLUTE MAXIMUM RATINGS

2 H HDLJIHHDL H HD H D JH H KH LH HG

PARAMETER	DEFINITION	MIN	MAX	UNIT
9,1	0DL L DJH D JH			9
9287	0DL DJH D JH			9
9)%	0DL IHHGEDF L DJH			9
9(1	0DL H DEHL DJH		9,1	9
93	0DL H J G L DJH			9
93 /	0DL H J GGHD L DJH			9
7-	- FL H HD H D JH			&
7 J	6 DJH H HD H D JH			&

(1) 6 H H EH G K H L HG GH E H0DL 5DLJ D FD HGH LEH H D H GD DJH 7KHGH LEHL J DD HHG I FL LGH IL 5HF H GHG2 HDL & GLL
(2) F H L L H L K GEHF HF HGEH HH 3 D G KH HG H HJ 9287 KH H : KH KH HG H L KUKH KD 9 KH D L & H /L L L EH H H KD HF KH=H H
(3) 2 HDL LKL KL D JHD LG H D H GH LEHGD DJH K JKHHF LFD HI D FHL J DD HHG LGH KH HDLJ D ELH H HD H D JH

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
9(6	+ D %G 0 GH +%0 H 16,-((&-6 HFILLFD L D L			9
	&KD JHG H LEH0 GH & 0 H 16,-((&-6 HFILLFD L D L			9

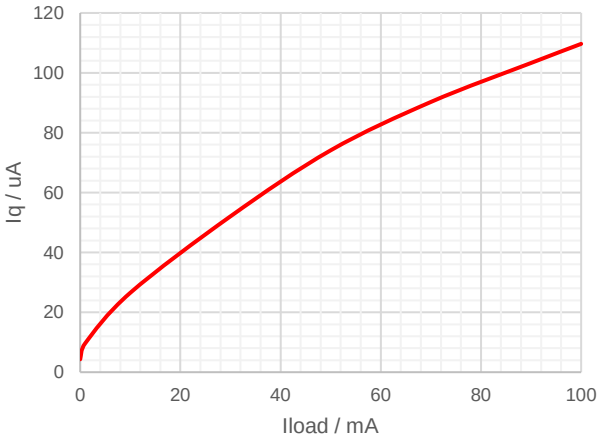
(1) -((&GF H -(3 DH KD 9+%0 D DIH D IDF LJ LKD D GDG(6 F FH
(2) -((&GF H -(3 DH KD 9&0D DIH D IDF LJ LKD D GDG(6 F FH

ELECTRICAL CHARACTERISTICS

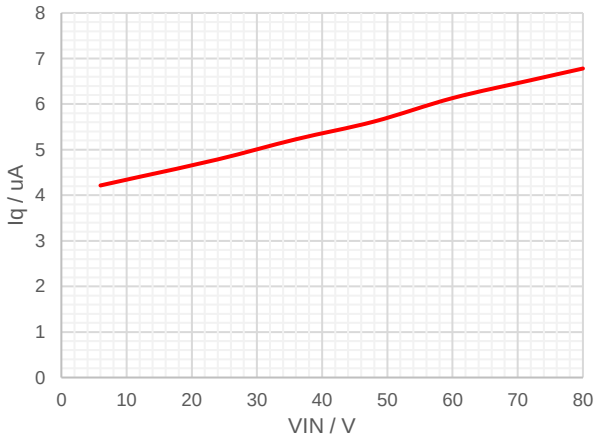
9,1 9287 9 &287) 7- & & LFD D HL H HG GH &

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
9,1	2 HDLJL DJH					9
989/2	9,1 89/27KHK G + HHL	9,1 LLJ				9 9
,6+ 1	6K G F H I 9,1 L	(1 9,1 9				
		(1 9,1 9				
,4	4 LH FH F H I 1 L	(1 I D DG 9,1 9 7- &				
		(1 I D DG 9,1 9 7- & &				
		(1 I D DG 9,1 9 7- &				
		(1 I D DG 9,1 9 7- & &				
Regulated Output Voltage and Current						
9)%	)HHGEDF DJHDFF DF	7- &				9
		7- & &				9
9287	/LH HJ DL	9,1 9287 9 9				9
	/ DG HJ DL	,				9
9 523	DJH	9,1 9287 9 ,				9
		9,1 9287 9 ,				9
,287	2 F H	9287 L HJ DL				
,2&	2 F H L L					
,2&)%	2 H & H) GEDF	9,1 9,1B+, + 9				
3655	3 H HHFL DL	9287 9 , I + &287)				G%
		9287 9 , I + &287)				G%
		9287 9 , I + &287)				G%
Enable and Soft-startup						
9(1B+	(DEHKJK KHK G					9
9(1B/	(DEH KHK G					9
9(1B+	(DEH KHK GK HHL					9
,(1B 9	(DEH L F H	(1 9				
766	6 I D L H					
Power Good						
93 B5	3 LLJ KHK G HFH DJH	9287 9287 120 KH 9287 LLJ				
93 B)	3 IDLJ KHK G HFH DJH	9287 9287 120 KH 9287 IDLJ				
9+<6	3 L K HHL					
93 B/2:	3 DJH	VOUT=0.8xVOUT(NOM),PG sink 100uA		76		9

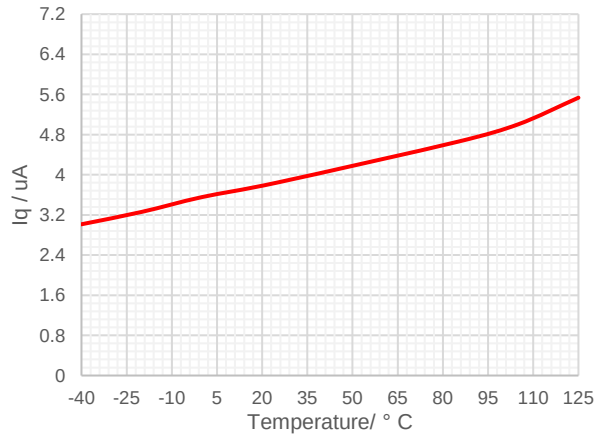
TYPICAL CHARACTERISTICS



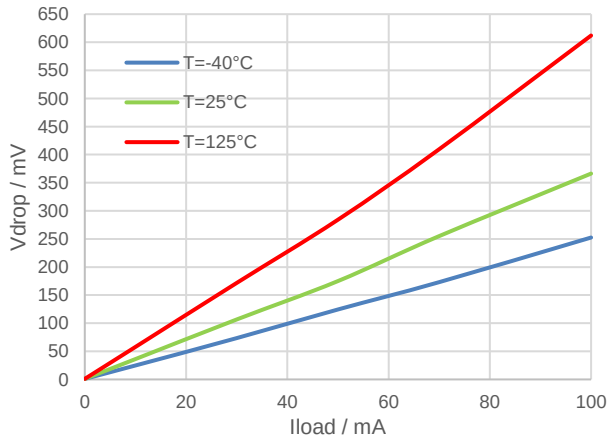
) LJ H 4 LH FH & H 2 & H



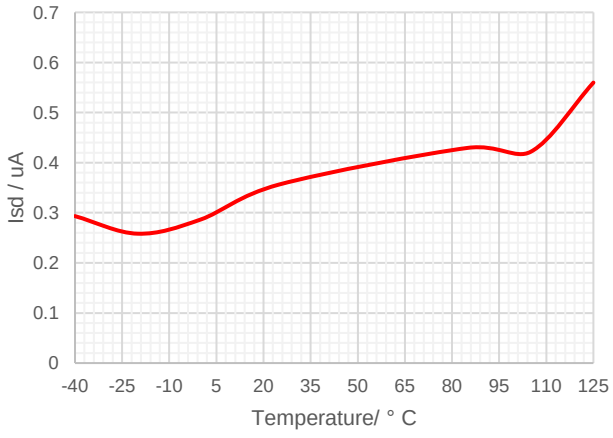
) LJ H 4 LH FH & H , 9 DJH 1 DG



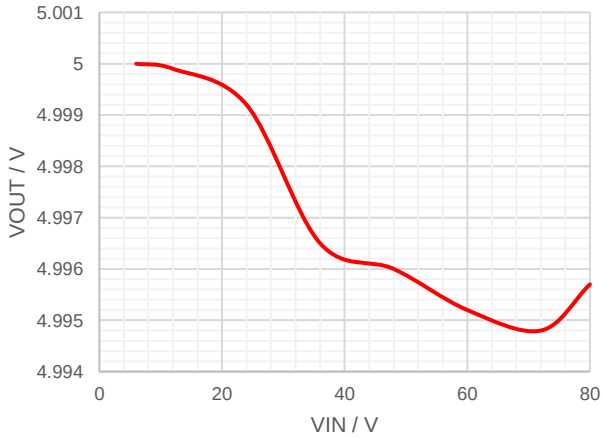
) LJ H 4 LH FH & H EtH 7H HD H



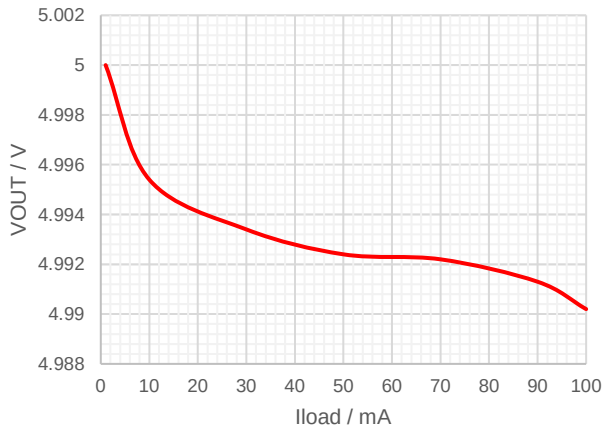
) LJ H 9 DJH 2 & H



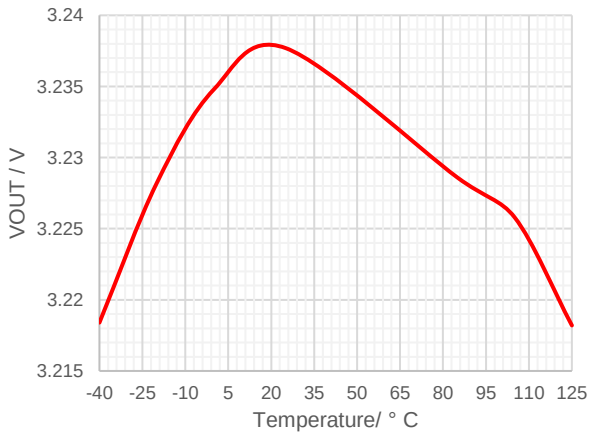
) LJ H 6K G & H EtH 7H HD H



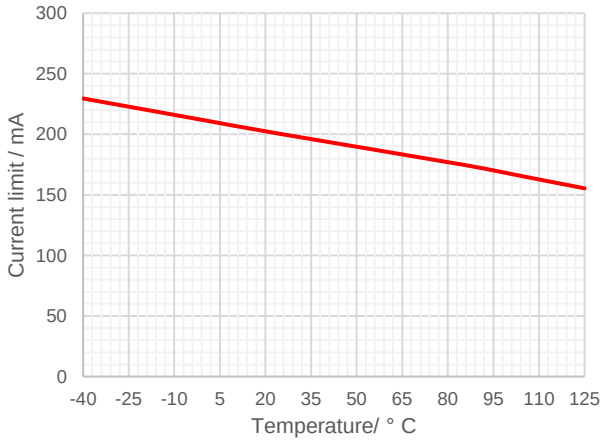
) LJ H 2 9 DJH , 9 DJH



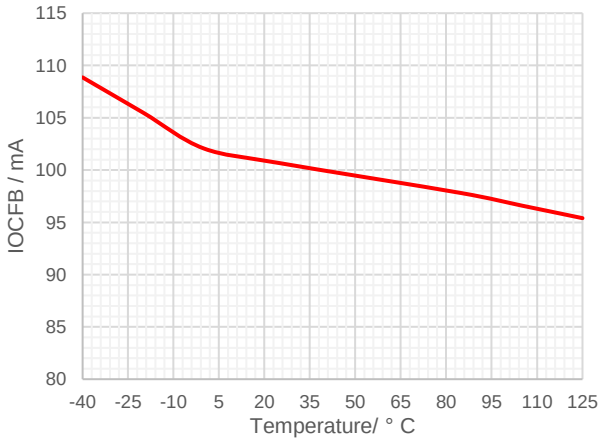
) LJ H 2 9 DJH 2 & H



) LJ H 2 9 DJH EILH 7H HD HD 9287 9



) LJ H 2 & H /L L EILH 7H HD HD 9,1 9



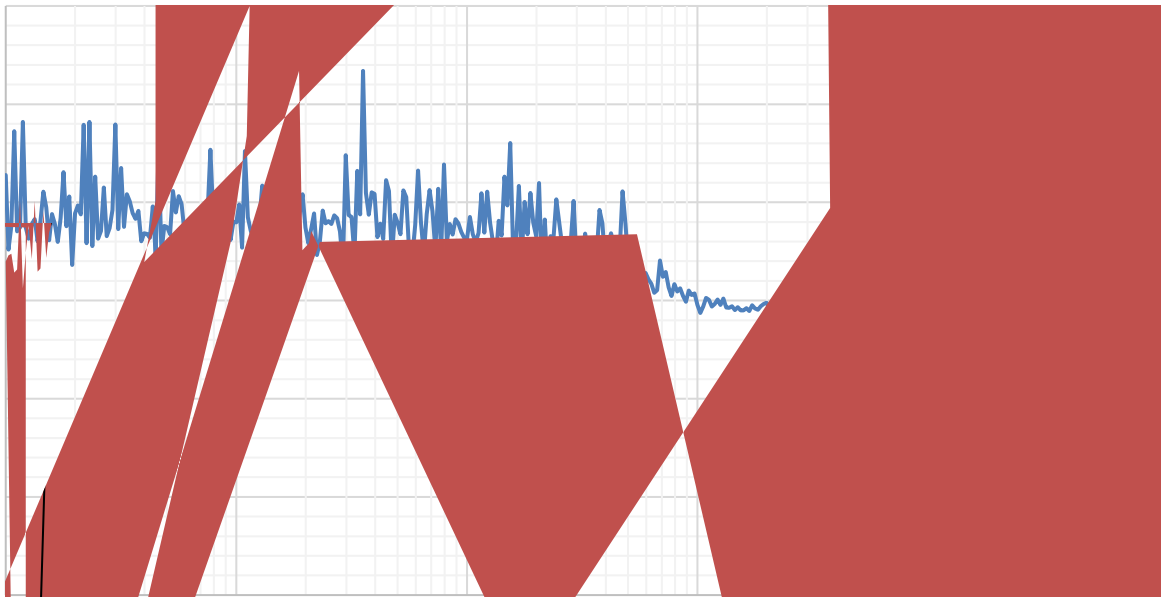
) LJ H 2 & H /L L EILH 7H HD HD 9,1 9

TYPICAL CHARACTERISTICS (continued)

)LJ H 3655) H H F
9287 9&I)&287),287

)LJ H 3655) H H F
9,1 99287 9&I),287

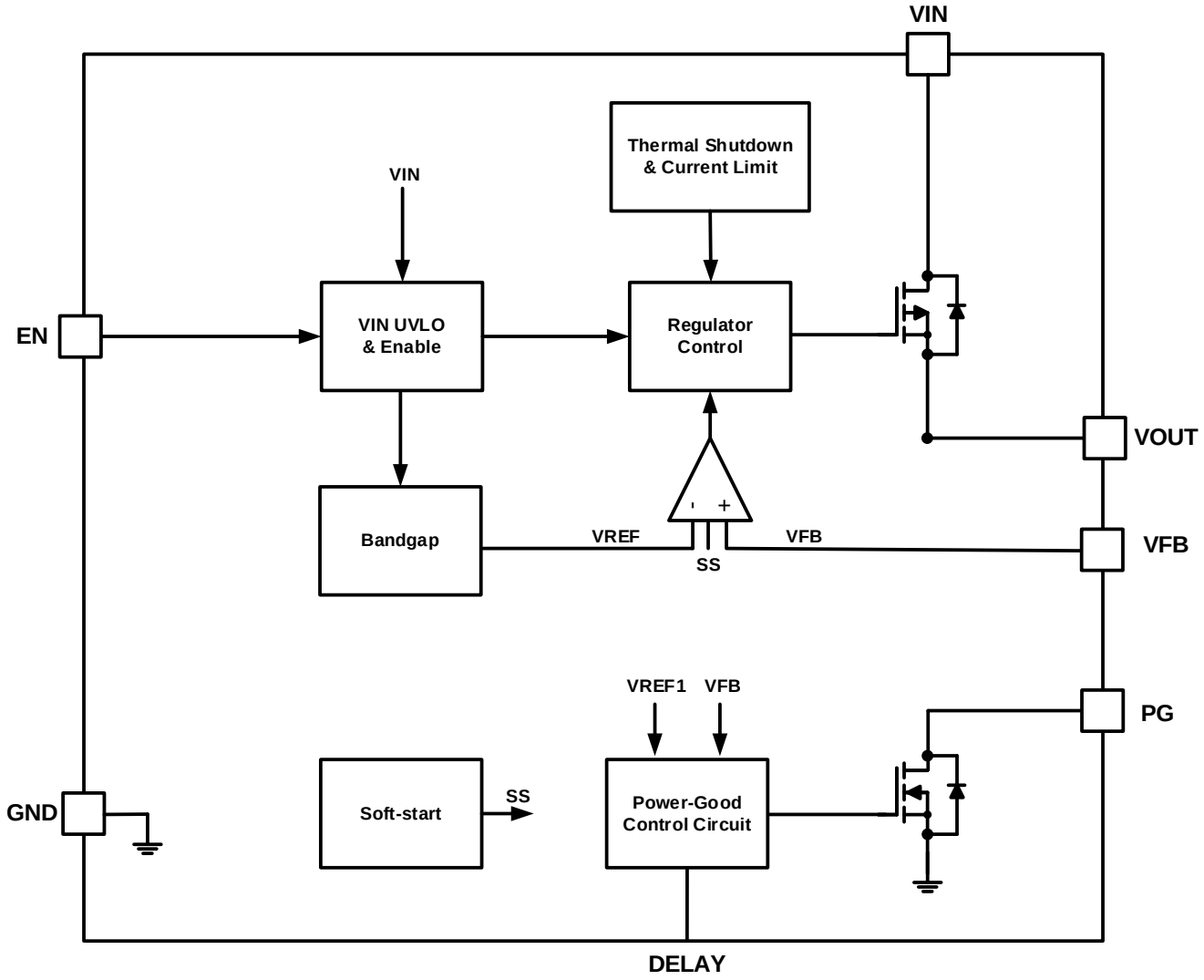
TYPICAL CHARACTERISTICS (continued)



)LJ H 3655) H H F
9,1 9 &I) &287),287

)LJ H 3655) H H F
9,1 99287 9 &I) &287)

FUNCTIONAL BLOCK DIAGRAM



)LJ H) FL D % F IDJ D I G 2 9H L

OPERATION

Overview

7KH 6&7 H LH G F D H LGH L DJH D JH L HD HJ D LK H LH FH F H 7KH H DJH HJ D HDHI 9 9 &L DJHD GF H LH FH F H D DG

7KH 6&7 H LH G F L DE H LK)) FD DFL D G) FH D LF FD DFL L HF H GHG L H D I D L HD LG DJH L KF H D G DJH H K G L J D

7KH 6&7 H LH G F D LGH H DE H F 3 H GIHD HD G J D DE H 3 H G GHD L H KLFK L H LDE H I KH D LFD L HHGL J H H FH F ILJ D L 2 KH HF L IHD H L F GH KH 9,1 L GH DJH F H F H HF L KD G K HF L D G KH D K G HF L

7KH 6&7 H LH G F LGH DG DE H H L I 9 9 ,I HHGD H DJH H L D H DF DJH L HD HIHH I HH F DF 6&7 DH

Enable and Under Voltage Lockout Threshold

7KH 6&7 H LH G F L H DE HG KH KH 9,1 L DJH L H DE H 9 D G KH (1 L DJH H FHHG KH H DE H K H K G9(1B+ 7KH GH LEH L GL DE HG KH KH 9,1 L DJHID EH 9 KH KH (1 L DJH L EH 9(1B/ , H D F H FH (1 L D KH GH LEH H DE H KH (1 L I D

) D KJKH H 89/2 K H K G F HF D H H D H L GL LGH 5 D G5 I 9,1 1 K L)LJ H 7KH 89/2 LL J D GID L J K H K GFD EH FDF DHGE (DL D G(DL H HF L H

: KH H

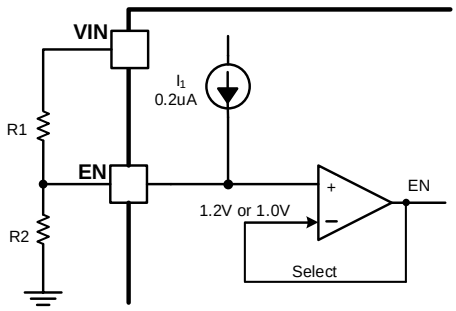
9,1 LH 9L LH K H K G H DE H KH GH LEH

9,1K 9L K HH L K H K G

, D GF GEH HJ HF HGL KH FDF DL

9(1B+ 9

9(1B/ 9



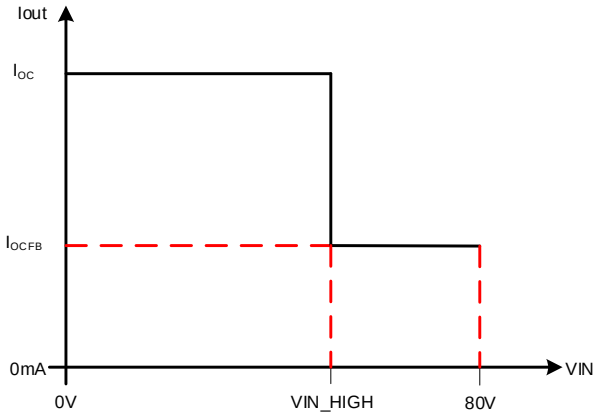
)LJ H 6 H 89/2 E H DE H GL LGH

Regulated Output Voltage

: KH KH L DJH L K JKH KD 9287120 9523 L L KH HJ D HG ED HG KH H L HG DJH H L : KH KH L DJH ID EH 9287120 9523 L DF KH L DJH L KH G DJH ED HG KH DGF H : KH KH L DJH G EH 89/2 K H K G KH HH G H DHG2 7K H K G

7KH DJH L HJ DHG KH KH GH LEH L L F H L L : KH D F H L L H H FF KH HJ D EHJL KHD EHFD H I KHL F HD HL H GL L DL ,I KH D K G L LJJH HG KH GH LEH II I H KH GH LEH F G KH L H D KH D K G FLF L KH GH LEH EDF ,I KH F H ID F GLL H L KH GH LEH F FH EH HH F H L L D G KH D K G

: LK KH H F H VIN_HIGH Control IHD H KH 6&7 H LH G F G EH H E D G DIH KH H F H ID D G K L J H H FF % L D H LH KH D L DGL J F H K G EH D H KD ,2&)%G L J D 7KH FKD DF H L LF L K L KH I L J I LJ H



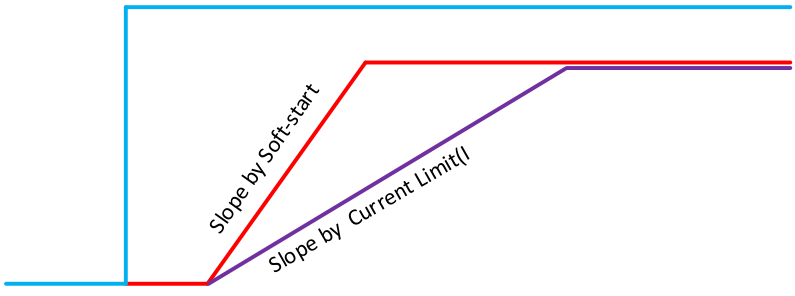
)LJ H & H /L L LK) GEDF)HD H

Internal Soft-Start

7KH 6&7 H LH G F L HJ DH D L H D I D FLF L KD D KH HH H FH DJH I H 9 HH H FH DJH L ,I KH (1 L L HGEH 9 / 2 L EH K II D G KH L H D I D H H 7KH I D D H H G L J K G G H KH D H DGL J

%H ILJ H K KH D D H D D FD DFL D G DJH FD DFL : KH FD DFL L D I H D H) KH H I 9287 L L LE I D : KH FD DFL L DJH I H D H) KH H I 9287 L L LHGE F H L L ,2& D 9,1 VIN_HIGH D G KH H I 9287 L L LHGE F H L L ,2&)% KH 9,1 VIN_HIGH

, 6&7 H LH G F LFD 7 L D G LFD ,2& L D G LFD ,2&)%L F G H KHI L J I DI L LID D L HFDF DL



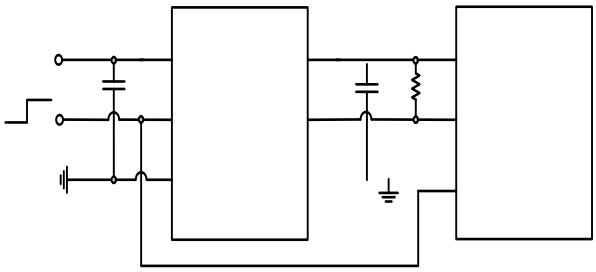
)LJ H 6 I D : D H 2 &D DFL

Power-Good and Power-Good Delay

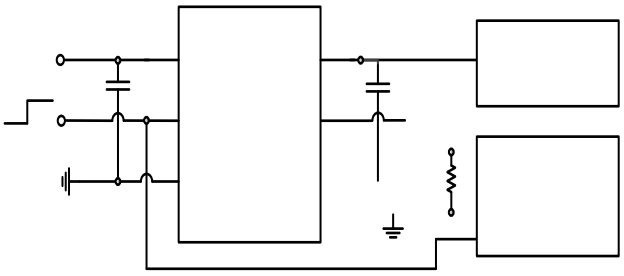
7KH H J G 3 L L D H GDL D GFD EHF HF HG D 9 H DL K JKD H H D H L 7KH 3 L KLJK L HGD FH KH 9287 L J HDH KD KH 3 L KH K G 9$_{3\ B5}$ 9$_{287\ 120}$,I 9287 G EH 9$_{3\ B)}$ 9$_{287\ 120}$ KH H GDL D G KH 3 ,I DJH L LJ L HHGHG KH 3 L FD EH HI I DL J F HF HG 1

,I KH H J GGHD L HL H JKI HD LFDL F GF HF DH H D FD DFL I (/ < L 1 KL FD DFL L FKD JHGI 9 9 E KH (/ < L F H , $_{(/<}$ D GJH HDHH DGHD L H. When C_{DELAY} is used, the PG output is high-impedance when V_{OUT} exceeds V_{IT}, and V_{DELAY} exceeds V_{REF}. The power-good delay time can be calculated using: $t_{DELAY} = (C_{DELAY} \times V_{REF})/I_{DELAY}$. For example, when C_{DELAY}= 10 nF, the PG delay time is approximately 12 ms; that is, (10 nF × 1.2V) / 1 µA = 12 ms.

7 H H H HDL I KH H J GIHD H DL DL 9,1 9 9,1B0,1 , D F HF L I 3 L FLF L LK KH D H GLUHH H DJH KH/ 2 9287 H H %H DH KHF HF L H D H



)LJ H 3 & HF HG / 2 2



)LJ H 3 & HF HG KH KH 3 H 6

%H ILJ H K KH D D G K G L DL KH H D G H G

KH L KHL DJH D LHI 9 / 2 L L K G EHFD H9,1 L EH L 89/2 KH K G D G DJHL 9

KH L KH9,1 DJH HDFKH 89/2 KH K G H H D G/ 2 D FKD JLJ I FD DFL 9287 LLJ HHGL GHL HGE L H D I D I FL

KH L KH9287 DJH HDFKH D KH9,1 DJHD L LH ID H D G/ 2 JH L G HJL 7KH GLUH H FHEH HH 9,1 D G9287 L KHG DJH

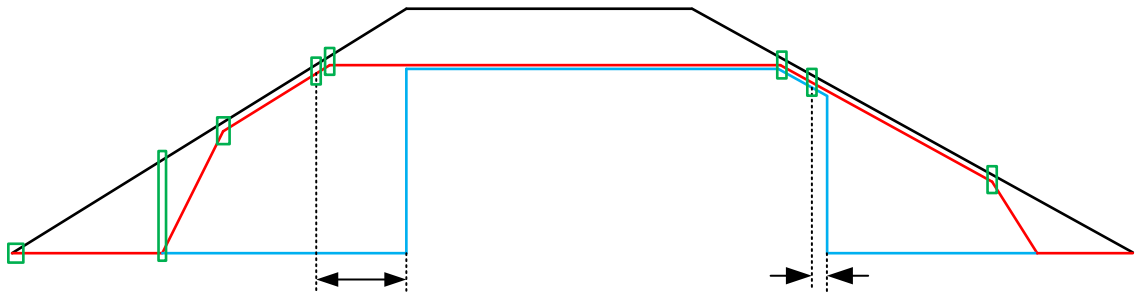
KH L KH9287 HDFKH 3 KH K G 9$_{3\ B5}$ 9$_{287\ 120}$ D GI KL L / 2 F KH H J GGHD L H IH KL GHD KH 3 L LH KLJK H H K LJ KD 9287 L

KH L KH9287 HDFKH L LD D H 9 H L D KH9,1 D EH KLJKH KD 9$_{287\ 120}$ 9$_{523}$ D G/ 2 JH L HJ DL HJL

KH L D KH9,1 DJH H G D G/ 2 H G HJL DJDL

KH L KH9287 G EH 3 KH K G 9$_{3\ B)}$ 9$_{287\ 120}$ D G/ 2 D F LJ KH H J GGHJ LFK L H KLFKILH ID 9287 GH K FD HGI H D HE LH DG D LH H H IH KL GHD KH 3 L K HG 9 H H KLJK LJK H IDL DH

KH L KH9,1 DJH L H KD L DJH 89/2 KH K G L 89/2 K HH L H H D G/ 2 J H L KH K G DH



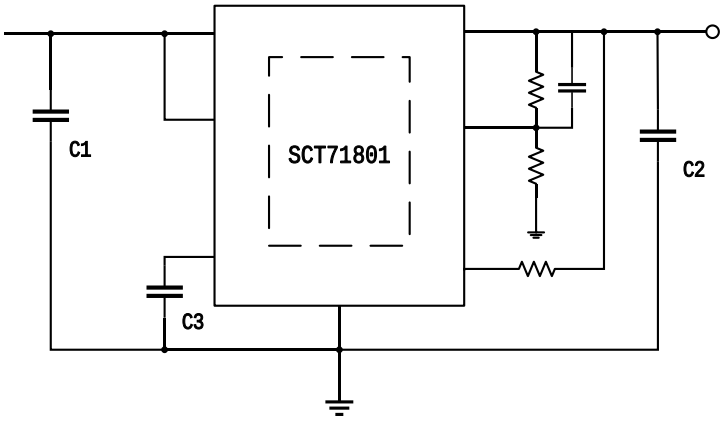
)LJ H 6D DG6K G (D H 6&7 6HLH

Thermal Shutdown

7KL GH LEHLF DH D KH D K G 7₆ FLF LD D HF L I HKHDLJ) F L D HDL KH FL H HD H K G H FHHG KH7₆ L L 7KH FL H HD HH FHHGL J KH 7₆ L L FD H KH II : G D H HD 0DK7K G

APPLICATION INFORMATION

Typical application 1:

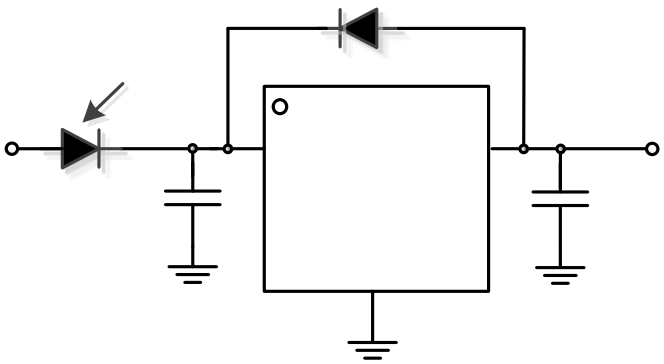


)LJ H 6&7 7 LFD LFDL 6FKH DLF

Design Parameters

Design Parameters	Example Value
, 9 DJH	9 1 D 9 9
2 9 DJH	9 9 9
0D L 2 & H	
2 &D DFL 5D JH &	)) HF H G)
, &D DFL 5D JH &	) HF H G)
3 H L I H J G 5	

Typical application 2:



)LJ H 6&7 7 LFD LFDL 6FKH DLF LK5H H H3 DL L GH

Design Parameters

Design Parameters	Example Value
, 9 DJH	9 1 D 9 9
2 9 DJH	9 9 9

0 D L 2 & H

Output Voltage

7KH DJHL H E D H H D H L GLLGH 5 D G5 L LED D LEDL FKH DIF 5HF H GHG 5 H L D FHL 8 HH DL FDF DH5

KH H

9 5( ) L KHIHHGEDF HIH H FH DJH LED 9

Table 1: Compensation Values for Typical Output Voltage/Capacitor Combinations

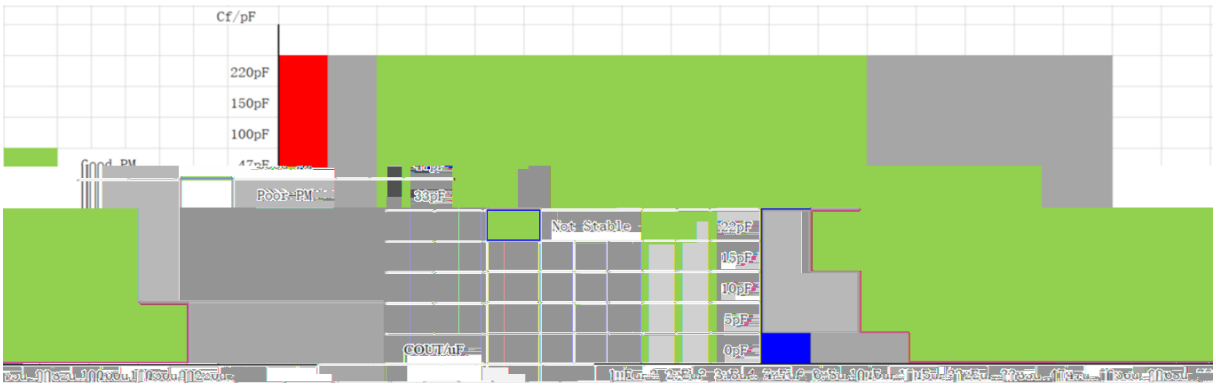
9 9	&287)	&I)	5	5	&287) (65 L D

Input Capacitor and Output Capacitor

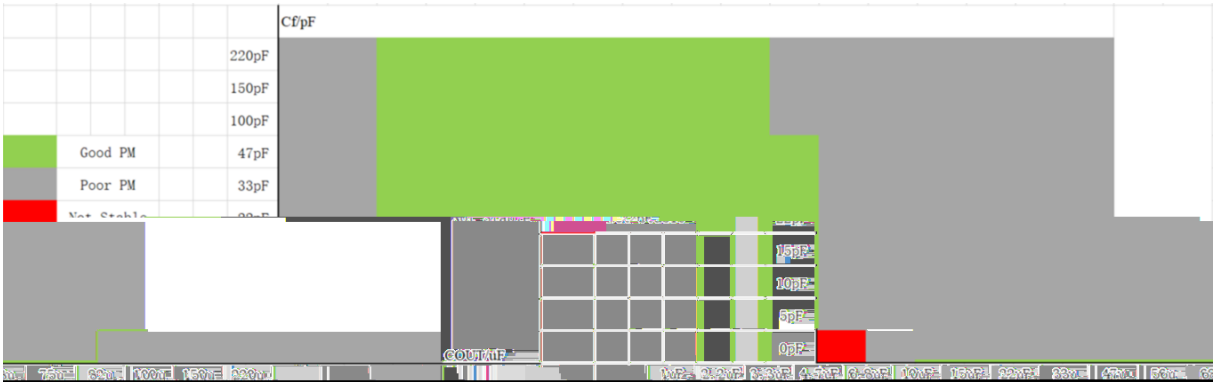
6&7 HF H G DGGL J D) J HD H FD DFL LK D) E D FD DFL L DD H D 9,1 L HH KH L DJH DE H L HHF LF FD DFL KH FD DFL LK KLJK FD DFLD FH L JJH HGI KH H H LK D JH DJH LH 7KH DJH DL J I KH FD DFL EH J HD H KD KH D L L DJH

7 H H DELL KH 6&7 G F H LH D FD DFL LK D L L HIHF LH FD DFLD FH D H I) G KH G F F G FD DFL D JH I)) D G LK D (65 D JH EH HH D G 6&7 HF H G HHF L J D; 5 ; 5 H)) FH D IF FD DFL LK (65 H H HD H D JH L H KH DG D LH H H

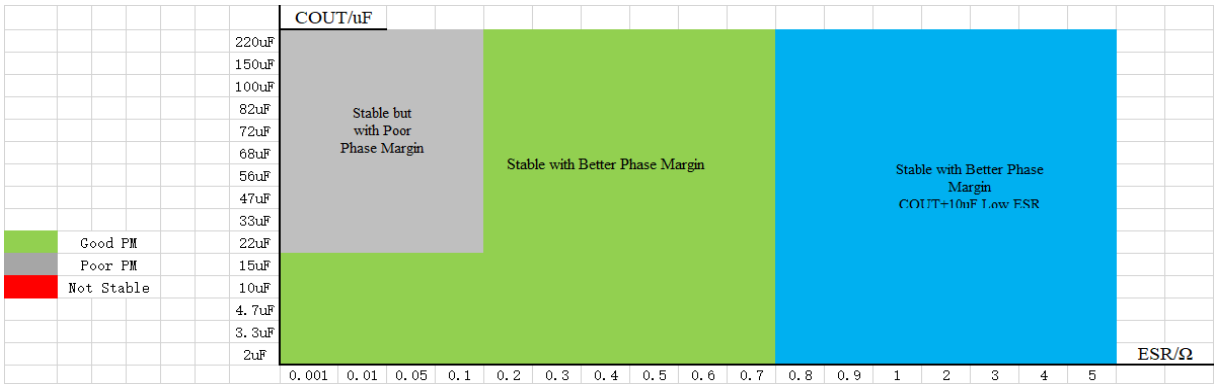
: KH L J D JH FD DFL LK KLJKH (65 H L I H D H) HHF LF FD DFL LK (65 H L L KH D LED L 6&7 HF H G DGGL J H D) (65 FD DFL D D H F HF L LK KH D JH HHF LF FD DFL KL L HL L DH KH GH K H K DJH FD HGE KH D JH (65 H L D GJH EH H DG D LH HI D FH



)LJ H 6&7)HHG) DG&D DFL HF H G5 9287 9



)LJ H 6&7)HHG) DG&D DFL HF H G5 9287 9



)LJ H 6&7 6 DELL 96 2 &D DFL

Power Dissipation and Thermal Performance

3 H GL LDL FD HGE DJHG DF KH/ 2 D GE KH F H I LJ K JK KH GH LEH HHG EH GL LDHG I KH FKL 7KH D L F L H HD HL GH H GH H GL LDL DF DJH KH 3&%D EH I HG& D H & D H KLF H D G KHD ELH H HD H

LJ D HDL / 2 F L H HD H K G H FHHG & H HL D H L GHHL DL I KH H LH I KH FKL 8 LJ EH H DL FDF DH KH H GL LDL D GH L DH KH F L H HD H

7KH H GL LDL FD EHFDF DHG LJ(DL %HFD H, 1 ,287 KH H 9,1 , 1 L(DL F G EHIJ HG

7KH F L H HD HFD EHH L DHG LJ(DL 5 - B(90 L KH F L D ELH KH D H L D FH ED HG F H 3&%9HIL KHD LFDL D GD IILFLH DJL L KH KH D GH IJ E KHI LJ HK GL HG FDF DH KH F L H HD H7-

5 - B(90 L DF LIFD DD HH D GGH H G D IDF FKD KHI LJ

3 H GL LDL

L H HD HI

3&%DHD

& H KHD L DHD

1 EH I KH D ID GH KH DF DJH

GDFH F H DFH H

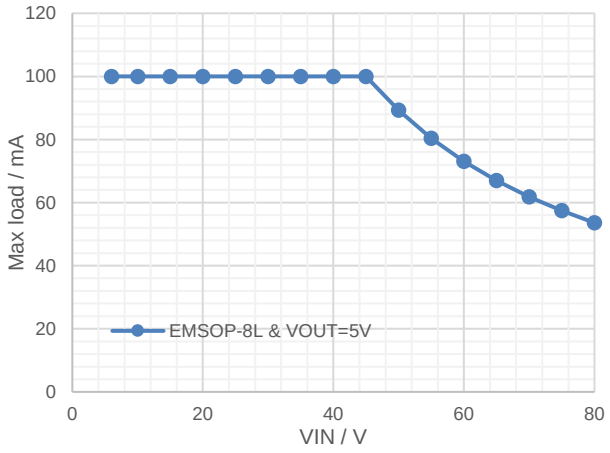
) KH6&7 G F KH D L D DEH H GL LDL I GUHH DF DJH D L HGL KH I LJ DEH D G KH H H DHED HG (90 E DG DJH H GL LDL L IJH KH D K G HF L D H HF GFDF DH KH5 - B(90 I GUHH DF DJH 7KHI LJ DEHL I HHH FHED HG (90 H HD H HD HH JK DJL KH GH IJ KH D HI D FH

7KH3&%LI DL I (90 D H & L H & LH

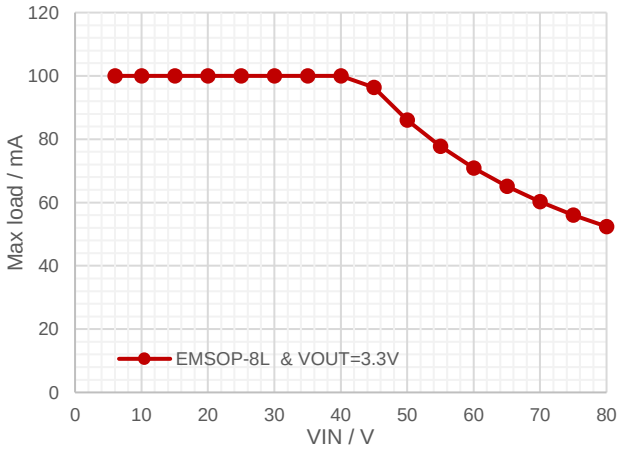
Thermal Performance of Different Packages Based on EVM Test

Package	Max Allowable PD (W) (Not Trigger TSD,VOUT=5V)	Max Allowable PD (W) (TJ≤150)	R JA_EVM (℃/W)
(0623 /			

THERMAL CHARACTERISTICS



)LJ H 0DL 2 & H , 9 DJH 9287 9 IGLWHH DF DJH 7. 76 B5



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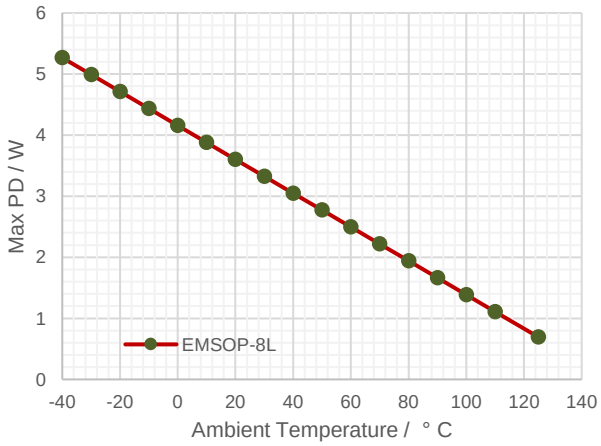

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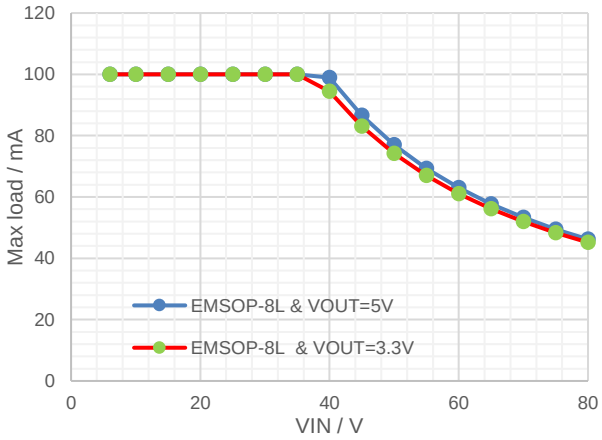

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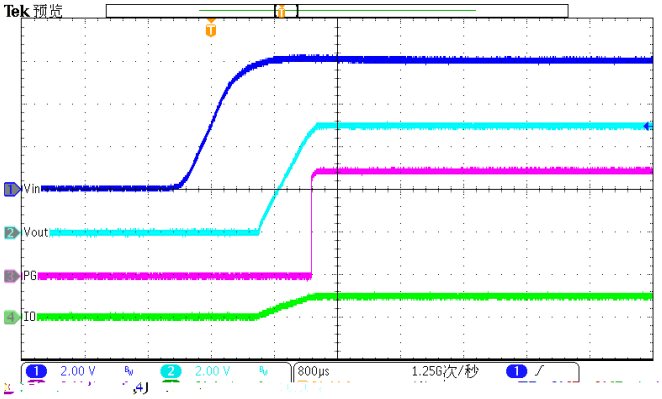
Application Waveforms

9L 9 9 H KH LH HG



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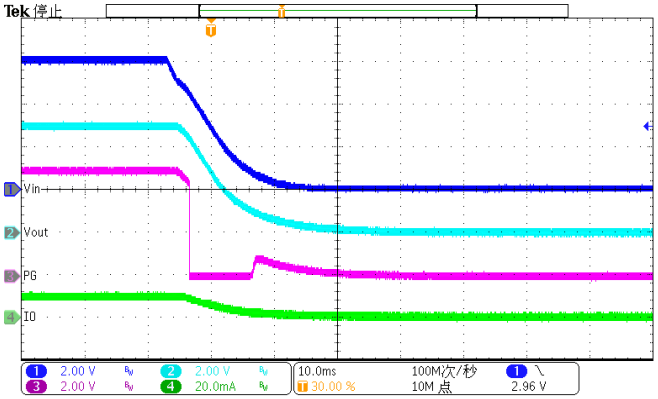

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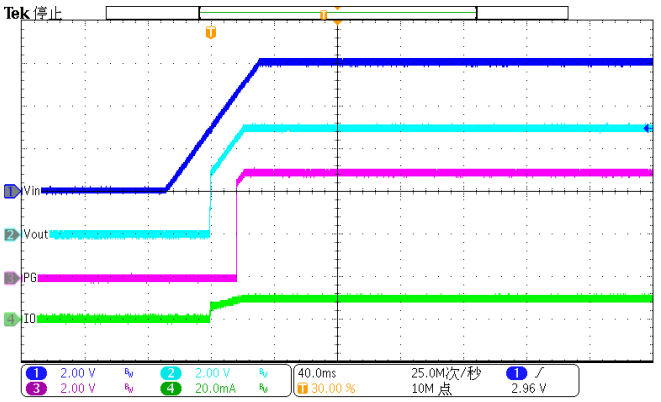

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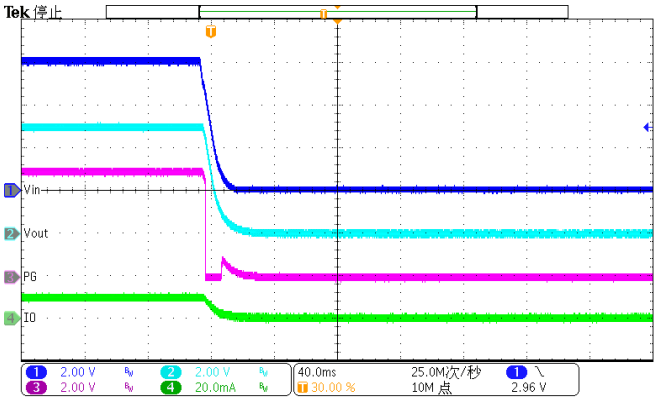


)LJ H . 6 3 HG 3 L HG 9287

)LJ H & &/ DG7 D LH

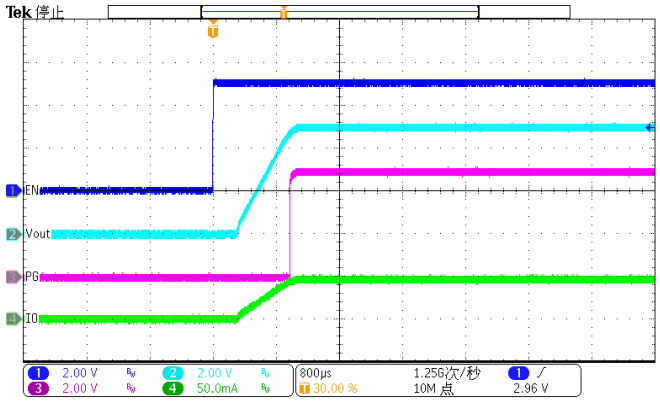
9287 9

)LJ H & &/ DG7 D LH

9_{287} 9

Application Waveforms(Continued)

9L 9 9 H KH LH HG



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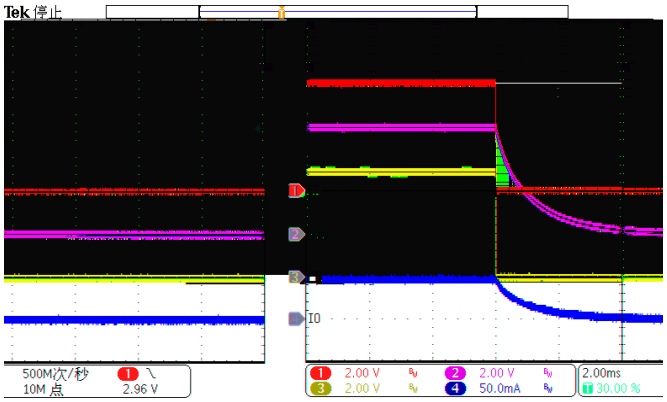
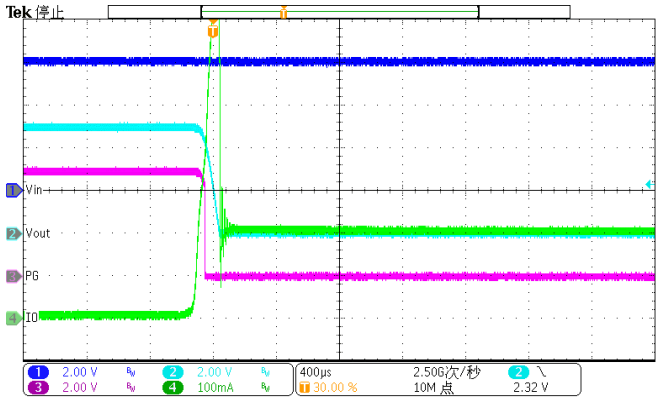


)LJ H LDEH , DG



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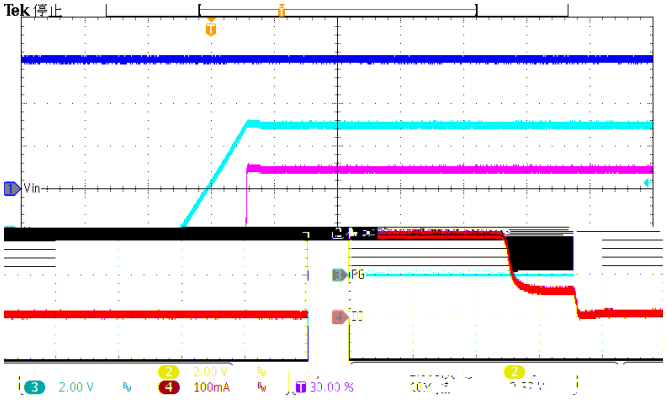

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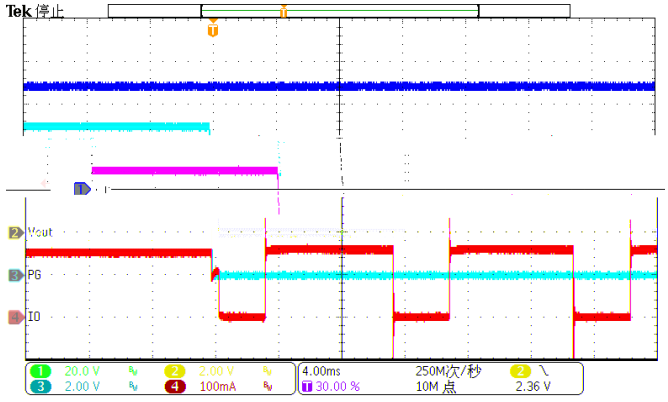
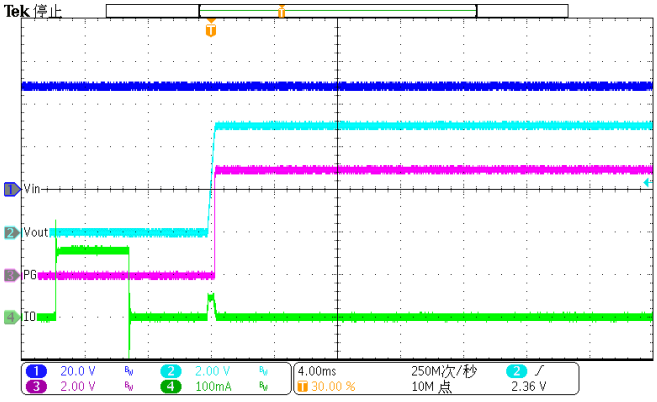


)LJ H (H2 H7H HD H3 HFL 9L 9

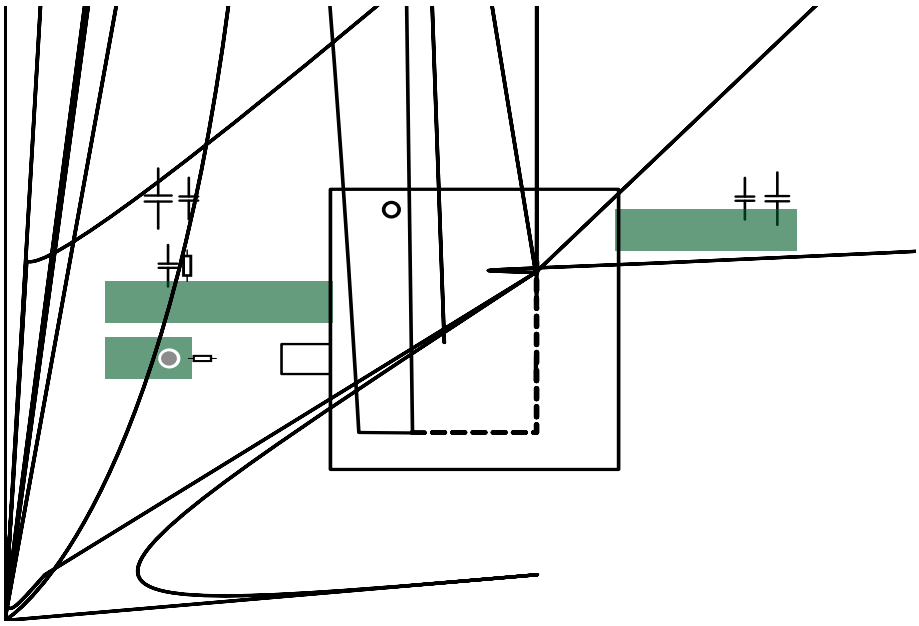


)LJ H (L2 H7H HD H3 HFL 9L 9

Layout Guideline

3 H 3&%D L DF LIFD I 6&7 DELL D LH HI D FHD GJ G HJ DL FKD DF H L IF) EH H H I KH HJ LGHL H D EH

1. % K L FD DFL D G FD DFL EH DFHGD F H KHGH LEH L D LE H
2. , L HF H GHG E D KH L L J G LK D) E D FD DFL 7KH D HDI HGE KHE D FD DFL F HF L 9,1 L D G KH 1 L I KH H EHD D D LE H
3. , L HF H GHG H LGH DFH H J K KIF F H HIJK L L LH, 5 G D GKHD GL L D L
4. 7 L H KH KH D HI D FH I KHGH LEH D G D L LH KHF H D KIJK D EIH H H D H 6&7 HF H G HDGL J KH F H GH KH KH D DG D ID D LEHD G DFL J H JK KH D ID KH F H GH KH KH D DG
5. ,I L J D JHHHF IF FD DFL LK KIJK (65 H L 6&7 HF H G DGGL J D) (65 FD DFL D D H F HF L LK KH D JHHHF IF FD DFL

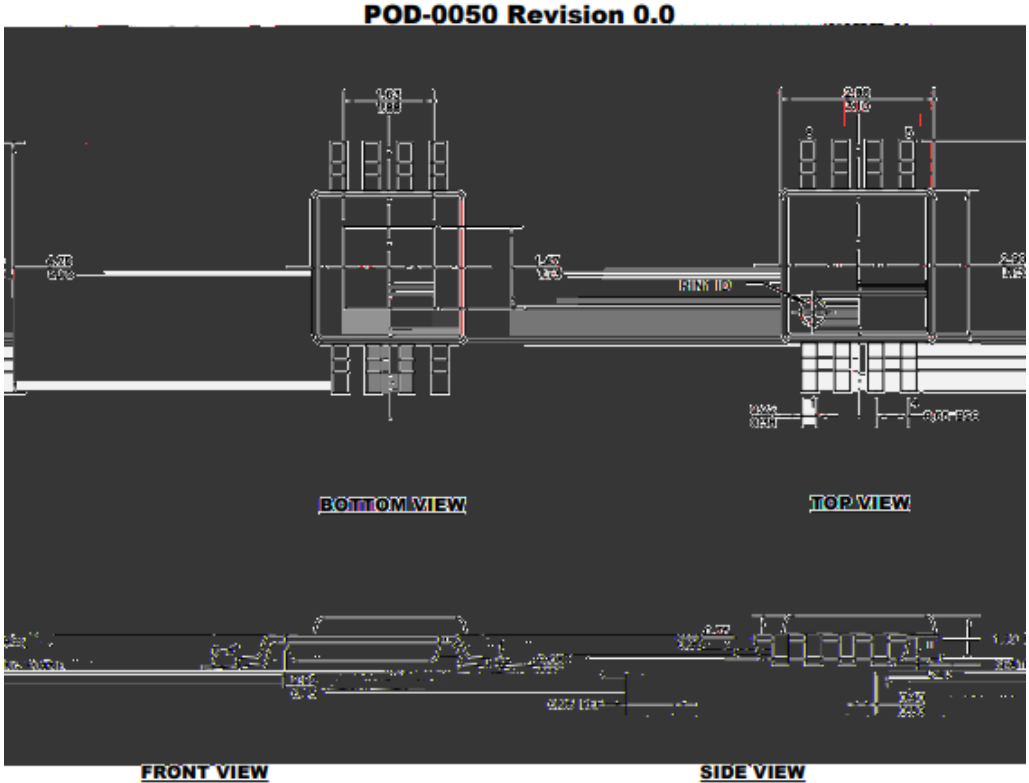


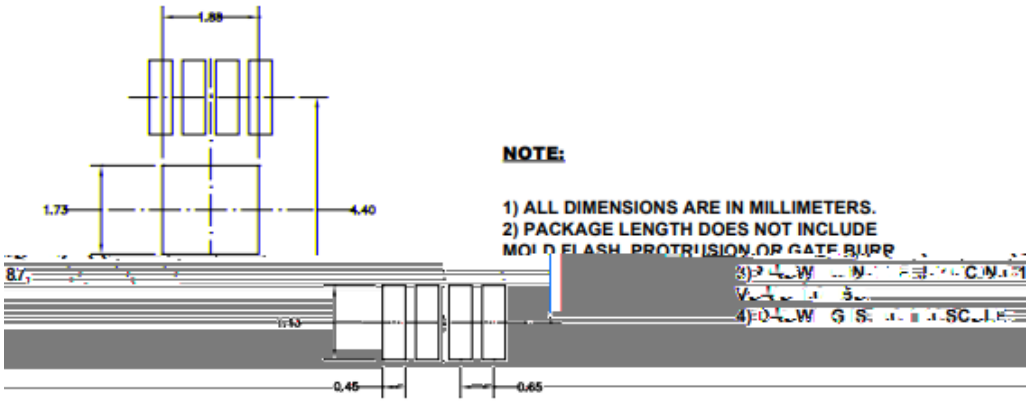
)IJ H 3&%/D (D H

SCT71801A00MTER

PACKAGE INFORMATION

PACKAGE OUTLINE DRAWING FOR MSOP8L-EP
POD-0050 Revision 0.0





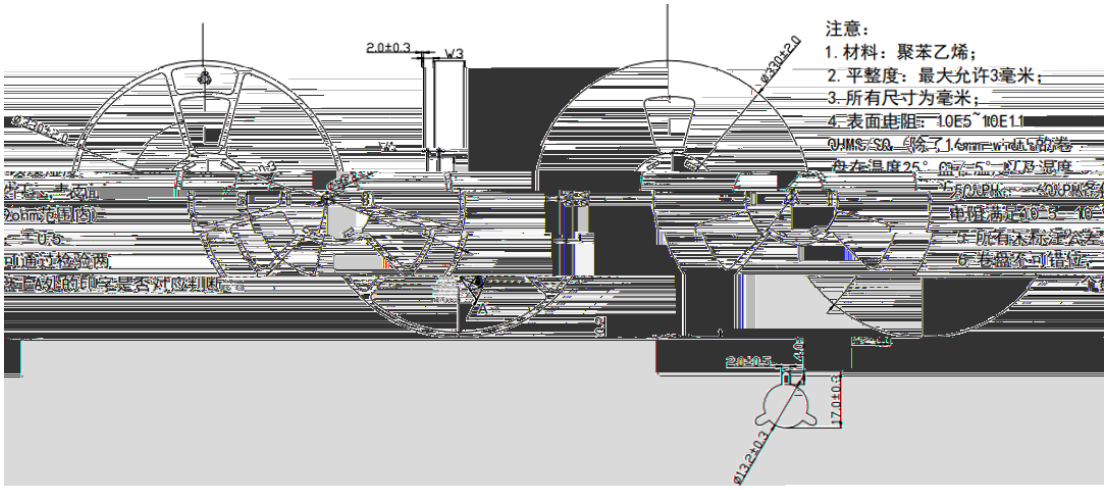
RECOMMENDED LAND PATTERN

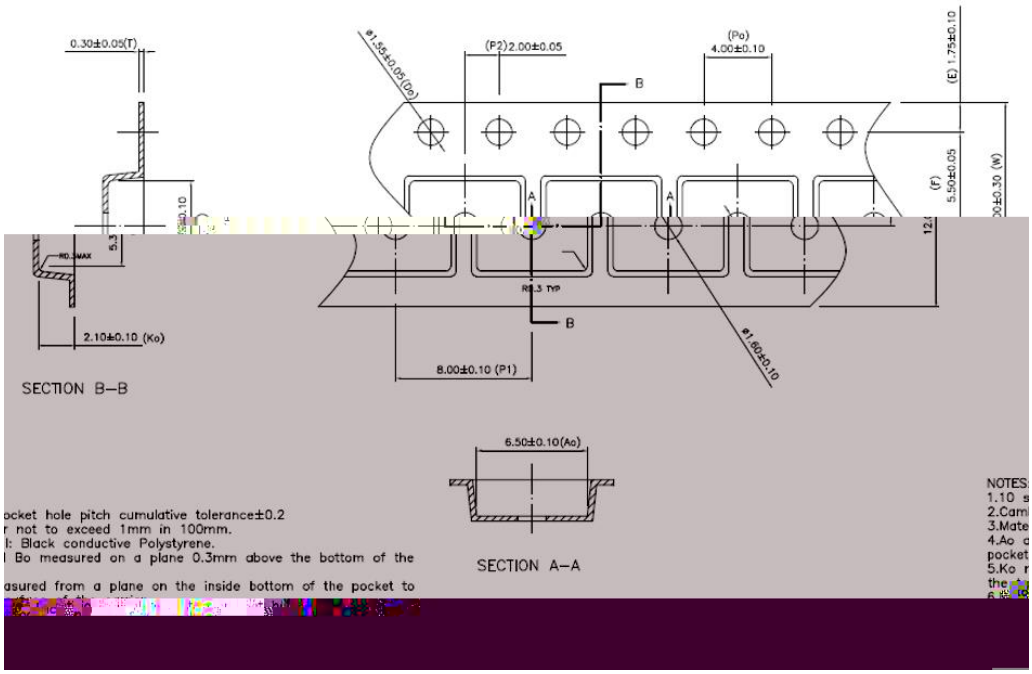
(0 6 2 3 / 3DF DJH 2 L H L H L

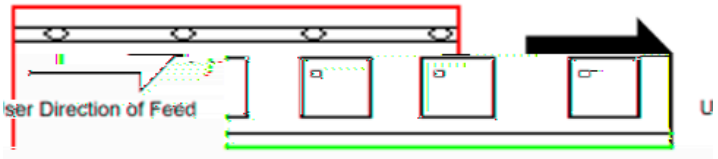
NOTE:

1. D L J HG EH DGHD-((& DF DJH L H 0 2 D I D L
2. D L J FDH
3. L H D GL H L D H L L H H
4. 7KH D DG KD EH GHHG KHE D G
5. L H L I H HG DG E I DF DJH G L F GH GI D K
6. & DF 3&%E D GIDE LEDL I L L GH D HE H D FH EH HH KH L

TAPE AND REEL INFORMATION







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NOTICE: 7KH LI DL L KL G F H L EHF FKD JH LK LFH 8 H K G D D D GJ DD HH KH KLG D , H HF D 3 H LJK DH LI L JHG KH L HJ DL J 6LIF & H 7HFK J 6&7 G F L D D LFD L 6&7 L D HD HJD H LELL I D DLGD LFD L